VL-C780S/H/X
VL-C7400E
VL-C690S/H/X
VL-C6400E

SHARP TECHNICAL MANUAL

T80H6VLC780S/

VHS C (PAL)

CAMCORDER

For VL-C780S/H/X VL-C7400E VL-C690S/H/X VL-C6400E

CONTENTS

SHARP CORPORATION

VCR SECTION

1. DESCRIPTION OF SERVO AND SYSTEM CONTROLLER CIRCUIT

1-1. Outline

Servo circuit VL-C780/C690 detects the speed error and phase error signals from the drum and capstan and filters the error signal by means of software. consisting of 1 chip as a system controller servo. (IC801)
Further, the system controller section has additional specifications such as remaining tape measurement, compatibility with rotary erase head (full erase head less), distinction of clogging, recording search, control of character display IC, and data transfer to camera microcomputer.

1-2. Description of servo section operation

The servo section is composed as shown in the servo block diagram, comprising phase comparison of drum and capstan motor, speed comparison, phase system filter, and speed system filter as software in the system controller IC (IC801).
The system controller IC mixes the phase system and speed system error signals and outputs as PWM signal. The secondary system LPF is externally installed in order to eliminate the carrier components of such signal, eliminating ripple components of PWM signal and taking out as DC signal.The signal is compared to the chopping wave of approx. 200 kHz, switches the transistor thus generating the drive voltage for the drum motor and capstan motor, smoothes it and inputs in each motor drive circuit. It causes the drum motor and capstan motor respectively to rotate.The motor outputs FG (PG) signal respectively, which is fed back to the system controller IC.

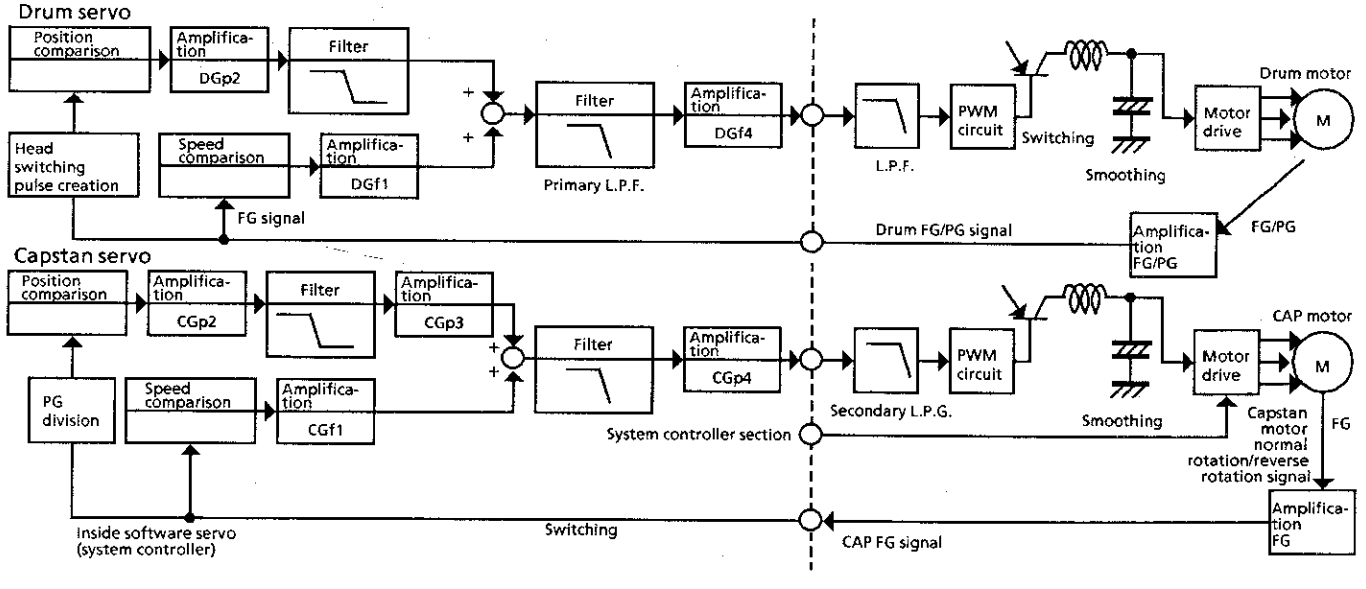


Figure 1-2. Servo Block Diagram

1-3. Servo reference data

		Capstan	Drum	REF 25Hz
mode	SP/LP	FG (Hz)	FG (Hz)	FG (Hz)
REC	SP	1008.93	600.003	25.00
	LP	504.46		
ASB (Editing record-ing)	SP	1008.93	600.003	25.00
	LP	504.46		
VSF	SP (*3)	3056.11	605.817	25.24
	LP (*3)	1520.67	602.889	25.12
	LP (*7)	3582.71	608.745	25.36
VSR	SP (*3)	2969.58	588.692	24.53
	LP (*3)	1499.03	594.308	24.76
	LP (*7)	3464.87	588.772	24.53
STI LL	SP	———	597.136	24.88
	LP	———	598.568	24.94

1-4. Arrangement of terminals

No.	name	IO	Terminal name	Circuit	Description	Initial
1	CLRO	I	DRUM PG	OPEN	Drum PG signal input	Z
2	SI	I	SLV DATA		Serial data input	
3	SO	O	SYS DATA	CMOS	Serial data output	
4	SCK	I	CLK	OPEN	Serial clock input	
5	NMI	I	TRIG	OPEN	Operation stop mode cancel pulse input	
6	P21	I	DEW L		Dewing detection input. Dewing = Low	
7	P22	I	SUP REEL		Supply reel pulse input	
8	P23	I	TUP REEL		Winding reel pulse input	
9	CT110	I	CAP FG		Capstan FG signal input	
10	CT100	I	DRUM FG		Drum FG signal input	
11	CT111	I	PB CTL		Playback CTL signal input	
12	CLR1	I	COMP SYNC		Composite sync signal input	
13	PTO00	O	H.SW.P	CMOS	25 Hz head switching pulse output	Z
14	PTO01	O	FALSE V		Pseudo-sync signal output in special playback (VSF, VSR, STILL)	
15	P32	I	DOC L		Video head clogging detection input	
16	PTO11	O	REC CTL		Record CTL signal output	
17	PWM0	O	DRUM PWB	CMOS	Drum motor control output	Low
18	PWM1	O	CAP PWM		Capstan motor control output	
19	AV_{SS}	—	GND		A/D converter reference GND terminal	
20	AV_{REF}	—	A/D 5V		A/D converter reference voltage terminal. Applies 5V in power-on.	
21	AN0	I	H.SW.P ADJ		H.SW.P. signal delay adjustment input	
22	AN1	I	TEST MODE		Test mode setting input	
23	AN2	I	BATT DET		Battery voltage input	
24	AN3	I	TAPE END		Tape end sensor input	
25	AN4	I	MECHA POSI		Mechanic position detection input	
26	AN5	I	KEY 1		Key 1 input	
27	AN6	I	KEY 2		Key 2 input	
28	AN7	I	KEY 3		Key 3 input	
29	RESET	I	RESET		Reset input (Low active)	
30	V_{DD}	—	5V		5V power source terminal	
31	X2	—			System clock oscillation Xtal terminal (12 MHz)	
32	X1	—				
33	V_{SS}	—	GND		GND terminal	
34	P00	O	SW 1	CMOS	Head 1 switching control output	Z
35	P01	O	SW 2		Head 2 switching control output	
36	P02	O	SW 3		Head 3 switching control output	
37	P03	O	SW 4		Head 4 switching control output	
38	P04	O	ROT ERASE		Rotation erase head control output. ERASE ON = High	
39	P05	O	CTL WRITE		High output in CTL recording	
40	P06	O	V REC H		High output in video recording	

No.	name	IO	Terminal name	Circuit	Description	Initial
41	P07	O	H.AMP.SW	CMOS	Drum switching pulse output	Z
42	P67	O	A FADE	CMOS	Audio fade control PWM output	Z
43	P66	O	V FACE		Video fade control PWM outout	
44	P65	I	RTC IN		Clock IC data input	
45	P64	I	SELECT		Operation mode selection input	
46	P63	O	EP H		SP/EP control output. EP mode = High	Low
47	P62	O	STILL H		Outputs HIGH in STILL mode	
48	P61	O	REMOTE LED		R/C Tally LED output. LED on = High	
49	P60	O	CTL ERASE		CTL erase control output. CTL ERASE on = High	
50	P57	I	POWER KEY	OPEN	Power key input. KEY push = Low	Z
51	P56	I	EJECT KEY		Eject key input. KEY push = Low	
52	P55	I	REC TIP	CMOS	Cassette tab detection input. Tab provided = Low	
53	P54	I	CASCON SW		Cassette controller detection input. Cassette controller down = Low	
54	P53	I	CAM/VCR		Camera/VCR switching input. Camera = Low	
55	P52	I	SP/EP		SP/EP switching input. SP = High	
56	P51	I	TRK UP		Tracking up key	
57	P50	I	TRK DOWN		Tracking down key	
58	P47	O	A MUTE	CMOS	Audio mute control output. MUTE on = Low	Z
59	P46	O	V MUTE		Video mute control output. MUTE on = low	
60	P45	O	EEL		EE control output. EE = low	
61	P44	O	RTC WR	CMOS	Clock IC WR signal	Z
62	P43	O	OSD/T DATA		OSD clock common data	
63	P42	O	OSD STRB		OSD IC STB signal	
64	P41	O	OSD/T CLK		OSD clock common CLK	
65	P40	O	POWER LED		Power LED light-up output	
66	CLO	O	CAPDIR	CMOS	Capstan rotation direction control. Reverse = Low	Low
67	V_{SS}	—	GND		GND terminal	
68	EA	I	5V		Access ROM selection input. Connected to 5V.	
69	P10	O	PCON H	CMOS	Outputs HIGH when VCR in on.	Low
70	P11	O	CAM CTL		Outputs HIGH when camera in on.	
71	P12	O	REC H		Outputs HIGH in REC mode.	
72	P13	O	PB H		Outputs HIGH in PB mode.	
73	P14	O	END LED		Tape end detection LED drive output. LED on = High	
74	P15	O	L/M FOR		L/M normal rotation control output. Normal on = High	
75	P16	O	L/M REV		L/M reverse rotation control output. Reverse on = High	
76	P17	O	CC READY		Cameral microcomputer serial transfer READY output	
77	V_{DD}	—	5V		5V power supply terminal	
78	P70	O	CAP MUTE	CMOS	Outputs HIGH in capstan mute mode.	Z
79	P71	O	RTC CS		CS of clock IC	
80	PTO10	O	REF 30Hz	CMOS	Outputs reference 25 Hz for digital video processing.	High

1-5. Condition of input signal

1. Power key

   It performs the following process to avoid malfunction due to noise.

   1) In power-on, it reads key levels 16 times after input of operation stop mode cancel pulse, and ignores external triggers unless two consecutive key depressions are detected

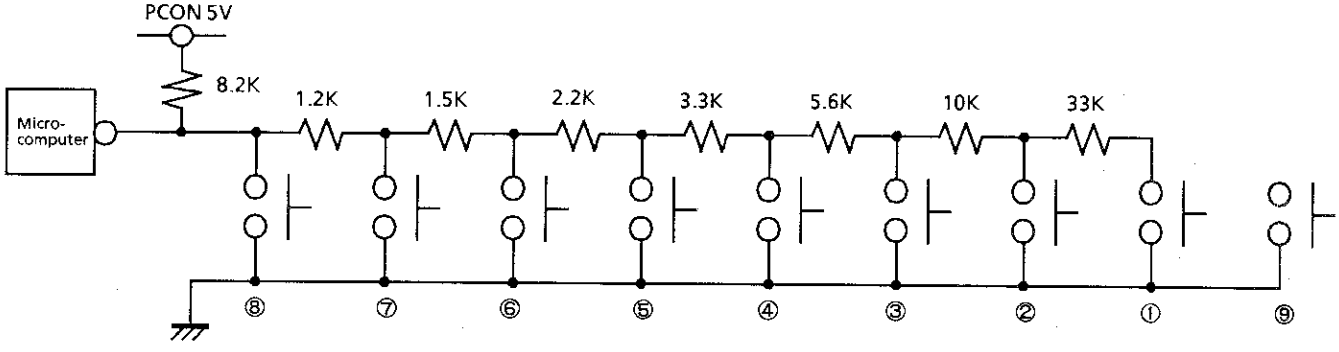
   2) It ignores the key for 200 msec after power-on.

2. Analogue input

   Each mode is distinguished by the voltage inputted through the resistance rudder circuit shown below.

   REC Start/Stop key, adopting a rubber contact switch, assigns an analogue input port (key 3), and judges depression in the voltage recognizing range the same as in the resistance rudder circuit.

   The rubber contact switch should have the hysterisis characteristics shown below because the resistance changes continuously.



Terminal No.	name	⑧	⑦	⑥	⑤	④	③	②	①	⑨
22	TEST	TEST8	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	
26	KEY 1	STOP	REW	PB	FF	PAUSE	FADE	SYNC S/S	SELF TIMER	
27	KEY 2	Calendar ON/OFF	Clock setting	Counter switching	Reset					
25	MECHA POSI	E SW		D SW	C SW	B SW	A SW			

PAL version has no sync S/S key

REC Start/Stop

Terminal No.	name	⑧	⑦	⑥	⑤	④	③	②	①	⑨
28	KEY 3	← ON								

1-6. Remaining tape alarming

1. The system clock of the microcomputer adopts 12 MHz X tal, and has better precision compared to conventional microcomputers. Therefore it does not adopt conventional remaining tape measurement system (Head Switching Pulse Count System), but measures the remaining tape by use of a system clock as a timer.
2. It measures the rotation cycle of a supply reel in REC mode, and displays an alarm when it is below the following (remaining tape 3 minutes or less):

   NTSC SP:2.737 sec/r, EP:7.660 sec/r

   PAL SP:3.792 sec/r, LP:7.296 sec/r

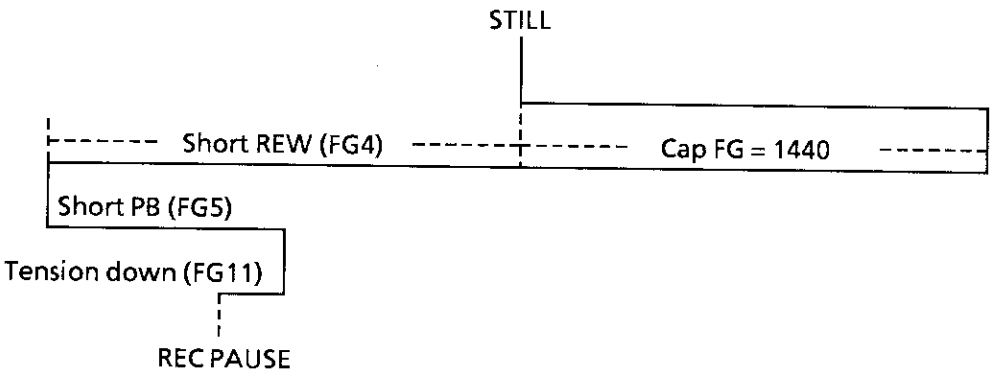
   It measures the remaining tape only in REC mode, not in other modes (such as recording search and playback).
3. When it measures the rotation cycle of both supply and rewind reels and calculates the actual tape thickness (tape thickness correction) based upon it, it can measure the remaining tape more accurately. However, it does not perform the tape thickness correction since no great error occurs.

1-7. Detection of battery voltage

1. The battery voltage is read in 131msec cycle and judged by an average of 16 times.
2. It is not performed during mode transmission where the voltage is likely to fluctuate.
3. The battery voltage is read in 22msec cycle only when power is turned on, and judged by an average of 8 times. When the average of battery voltage is 9.0V or below, power is turned off.

1-8. Recording search

1. Press the FF, PB, or REW key in REC PAUSE mode. Since the REW key is common with the REC REVIEW key, if it is pressed longer than 1 sec., the recording search mode is set.
2. As long as the FF key is pressed, the machine plays back in triple speed, and when the key is released, it plays back for a second in a double speed in forward direction, then enters the STILL mode.
3. As long as the PB key is pressed, the machine plays back in a double speed, and when the key is released, it enters the STILL mode.
4. As long as the REW key is pressed, the machine plays back in a triple speed in reverse direction, and when the key is released, it continues reverse rotation for 0.33 sec., then plays back in a double speed for 1 sec. in forward direction and enters STILL mode.
5. When the key is released, the STILL mode is held for 1 sec., then REC PAUSE is set.



1-9. Tally display

1. Tally display provides three types, display in view finder, main unit LED, and R/C LED, each displayed in the conditions below:

Operation	View finder display	Main unit Tally LED	R/C Tally LED
REC PAUSE	----- Lights up.	Lights off.	Lights off.
SELF TIMER standy		2Hz/4Hz flashes.	
Self-timer phase adjusting	>>>>> dancing	4Hz flashes.	Lights up.
REC phase adjusting		Lights off.	
REC		Lights up.	
Remaining REC tape alarming			1Hz flashes.
Other than the above		Lights off.	Lights off.

[Reference]
View finder display:
Lights up during REC PAUSE in camera mode. Dancing when PAUSE is canceled. Otherwise, no display.
Main unit Tally LED:
Lights up in recording in any mode. Flashes until self-timer recording starts. Otherwise, it lights off.
R/C Tally LED:
Lights up when PAUSE is canceled in a recordable condition in any mode. Flashes during remaining tape alarming in camera mode. Otherwise, it lights off.

2. Main unit Tally LED display is controlled by serial transfer of Tally flag to the camera microcomputer.

1-10. Tape alarm display

1. Tape alarm is displayed only in the camera mode.
2. When a tab-less cassette is placed in or the cassette controller is pressed down with no cassette, the "ERROR" flag (Unrecordable flag) is set and transferred to the camera microcomputer.

1-11. Self-timer

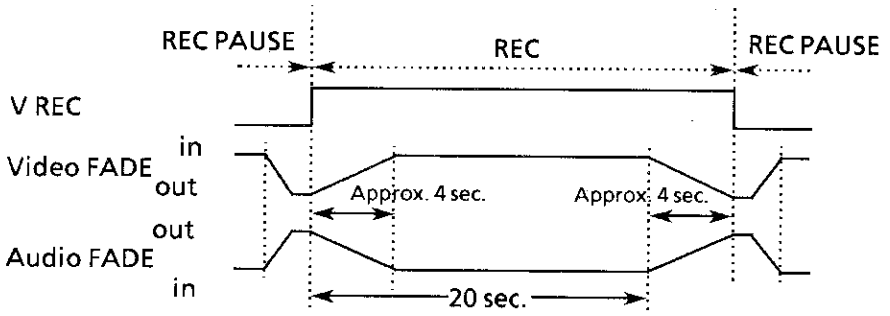
1. When the SELF-TIMER key is pressed in REC PAUSE mode, the SELF-TIMER mode is set.
2. Recording time is set by the number of times the SELF-TIMER key is pressed. It is shown below.The SELF-TIMER key is accepted in REC PAUSE mode or SELF-TIMER standby mode.

SELF TIMER off
↓ [SELF TIMER KEY push]
SELF TIMER mode ⓐ (Standby 10 sec., recording 20 sec.)
↓ [SELF TIMER KEY push]
SELF TIMER mode ⓑ (Standby 10 sec., continuous recording)
↓ [SELF TIMER KEY push]
SELF TIMER off

3. Recording is started in approx. 10 sec. after SELF-TIMER is set. When the SELF-TIMER key is pressed twice, recording is started in approx. 10 sec. after the second time. In standby mode, the Tally flag flashes in 2 Hz for the first 8 sec. and in 4 Hz for the remaining 2 sec.
   REC PAUSE is canceled in approx. 9 sec. after SELF-TIMER is set, but phase adjusting takes approx. 1 sec. so that actual recording starts in approx. 10 sec.
4. If FADE mode is set in SELF-TIMER mode, FADE-in/FADE-out is performed as shown in the drawing below.
5. REC Start/Stop, R/C Start/Stop, and FADE keys are accepted during recording, and other keys (including SELF-TIMER key) are not accepted.
6. SELF-TIMER, REC Start/Stop, R/C Start/Stop, FADE, EJECT, and POWER keys are accepted in SELF-TIMER Standby.

1-12. Fade-in/fade-out

1. Fade-in/fade-out is acceptable in the REC and REC PAUSE modes only.
2. Each time the FADE key is pressed, the FADE mode is called or cleared. During the FADE mode, "FADER" is displayed in the viewfinder.
3. In the FADE mode, fade-in occurs in the transition from rec pause to recording, and fade-out takes place in the transfer from recording to rec pause.
   Once the fade-in or fade-out is carried out, "FADER" in the viewfinder automatically disappears and the FADE mode is cleared.
4. There are two fade control outputs; V fade and A fade. These PWM output signals are reversed in polarity. The control signals are shown below. When the fade-in or fade-out has been carried out, it is automatically cleared. The chart below, therefore, shows an exmaple in which the FADE mode is called twice before and during recording.

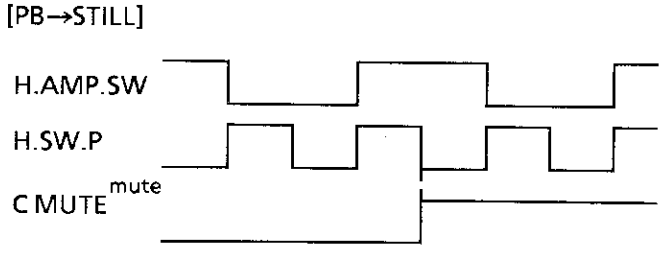


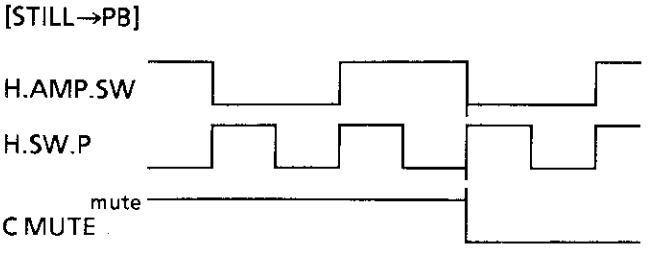
1-13. Process in resetting

Destination information is read in and power turned off. In reading in desitinations, the SELECT terminal is read in, and made effective if it provides the same level 16 times. The unit is for Europe when the level is H. (For Australia when the level is L.)

1-14. Special playback

1. Three types of special playbacks are available, i.e. VSF, VSR, and STILL.
2. False sync signals are outputted during special playback and for 1 sec. after transmission from special playback to playback.
3. In PB→STILL, the unit stops in sync with Head Amp. Sw. as shown in the figure below.
   Further, is STILL→PB, another mode is made hard to be set as shown in the figure belows.





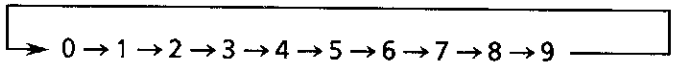
1-15. Clock IC control

Serial transfer with the real time clock IC (RTC-4523) contained in SRAM is performed, and clock processing and data back-up are performed. In entering the clock data, second digits are read in, and the whole clock is read in when they are changed, then back-up data are written in SRAM.

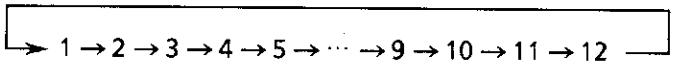
1-16. Clock setting

Pressing the clock setting key establishes the clock setting mode.
When the time is not set, the calendar switching key also establishes the clock setting mode.
In the clock setting mode, the TRACK UP key and TRACK DOWN key enable correction of date and time.
RTC-4523 is used for clock IC.
If setting of non-existing data of date is tried, control does not proceed to time setting but returns to initial setting.
Setting range of numerics
In the clock setting mode, the numerics change as follows every time the TRACK UP key is pressed.

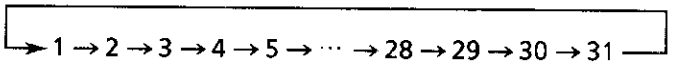
Year (set separately for upper and lower digits)



Month

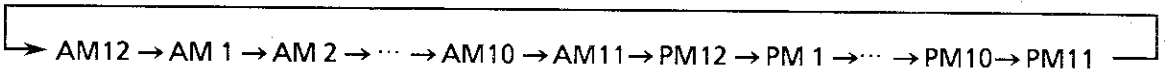


Day

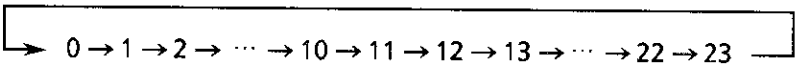


Hour

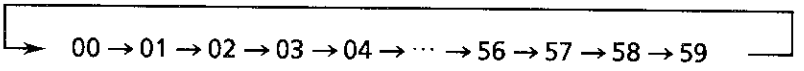
PAL destination selection L



PAL destination selection H



Second



1-17. Special function

The microcomputer has additional special functions necessary for service response and prototype examination.

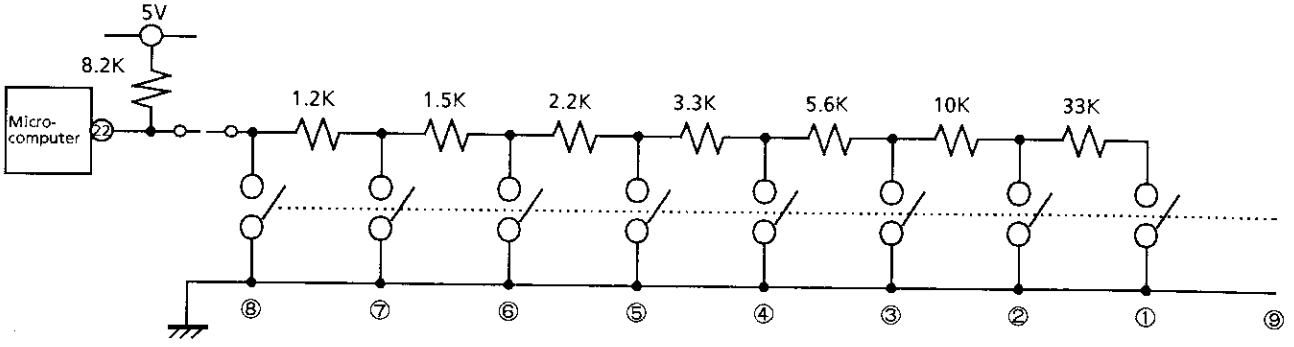
- Error message

When each sensor detects an error, the contents are shown in the counter display section in the view finder by the following codes.

Display	Record data of clock IC	Error contents
E007	1H	Capstan FG is not entered longer than 1 sec.
E011	2H	The next mechanical position is not detected though L/M is rotated forward longer than 5 sec.
E012	3H	The next mechanical position is not detected though L/M is rotated reversely longer than 5 sec.
E020	4H	Drum FG is not entered longer than 1 sec.
E025	5H	Rewind reel sensor error has occurred.
E026	6H	Supply reel sensor error has occurred.

- Test mode

Test modes of 8 types are allowed to be set depending on the voltage entered in pin (22).



SW No.	Test name	Test contents	Sensor on/off
1	Whole sensor off	Sensors are off except cassette controller SW, DEW, and battery detection sensors.	←
2	Substrate adjustment	L/M 5 sec. sensor is inhibited allowing checking of substrates without mechanism. (Do not connect mechanism in this mode.)	On except L/M 5 sec. sensor.
3	Battery adjustment	Adjustment error in the battery sensor is shown in the counter display in the view finder.	On except the battery sensor.
4	Error display	Past errors are shown in the counter display in the view finder.	All sensors are on.
5	Tracking display	Tracking data are shown in the counter display section, and the power LED flashes if the tracking is in the center.	All sensors are on.
6	Servo phase control inhibition	Phase control of capstan and drum is inhibited. (For measurement of closed loop of servo)	All sensors are on.
7	Adjustment mode for service	Adjustment mode of camera	(VCR stop)
8•[1]	Reel sensor off	Only the reel sensor is off.	On except the reel sensor.
9	Normal mode	Normal operation	All sensors are on.

Note-1. When the substrate is to be checked by means of the substrate adjustment mode, the microcomputer must be set as follows:
a. Ground the cassette SW input terminal.
b. Ground the REC TIP input terminal.
c. Connect a resistance of 23.8 k ohm between the TEST input terminal and the ground.
d. A jig is required which can generate capstan FG, head switching pulse, and reel pulse.

Note-2. When a cassette with a tab is placed in the camera mode, if the battery adjustment mode is set, REC is set automatically.

Note-3. Set the adjustment mode for service and follow the procedure below in adjusting a camera in service mode.

	Operation procedure	Display (▒ means flashing)
①	Increase or decrease the flashing numerics (hexadecimal digit) with the FF and REW keys to select an address to be adjusted. (Address in initial condition is 30H.)	ADJ ▒2C▒
②	When PB key is pressed, data is read out of the specified address. (Read out the data by READ command from the camera microcomputer.)	ADJ 2C A3
③	Increase or decrease the data by the FF and REW keys for adjustment. The data display section flashes. (The data is outputted to the camera microcomputer by DAOUT command.)	ADJ 2C ▒72▒
④	When the PB key is pressed, data is written in the specified address. (The data is outputted to the camera microcomputer by WRITE command.)	ADJ 2C 72
⑤	When the STOP key is pressed in the state ② or ④, the state ① is recovered.	ADJ ▒2C▒

If the FF or REW key is pressed continously longer than 0.3 sec., a repeat mode is set. The cycle of repeat is 100 msec, and in data setting, the data is changed by ± 4 when the key is pressed two more seconds.

- Auxiliary key input

The microcomputer enables direct key entry in VCR mode system provided for the camera microcomputer, not through data transfer from the camera microcomputer, so that it can perform basic operation check without being connected to the camera microcomputer.

Auxiliary key entries are assigned to the empty levels in the key 2 and 3 entries.

The keys with ▒ are for auxiliary entries in the table below.

name	⑧	⑦	⑥	⑤	④	③	②	①	⑨
KEY 1	STOP	REW	FF	PB	PAUSE	▒FADE▒	▒SYNC▒ ▒S/S▒	▒SELF▒ ※1 ▒TIMER▒	

2. VIDEO CIRCUIT

2-1. Features

(1) Y/C 1-chip IC

This model performs recording and playback process of Y and C in a single IC, which used to be performed in a separate IC, realizing simplification of a circuit. Further, the filters can be reduced by incorporating Y-LPF, etc. By the way, the Y/C 1-chip IC is also compatible with HQ as it was before.

(2) Video output circuit

The video output circuit has a zone signal mixing function in addition to conventional functions such as monitor output, view finder Y output, and non-record character mixing of the counter, alarm, etc.
Therefore, a new IC is adopted as an output IC in order to
take in these functions.

2-2. Flow of record Y signal

Y-signal outputted from the camera section is supplied to pin (3) of connector BG. First it is inputted to pin (1) of IC202 to mix the record characters. The record characters are created by switching the internal switch of IC202 with Y-signal by use of two types of pulse signals, and outputted from pin (7) as trimmed characters. It is then supplied to pin (1) input of IC201, i.e., AGC AMP. The signal entered in AGC circuit is divided into two inside IC201. One of them, passing through the sub-clamp circuit, MUTE circuit, and AMP as EE signal, is outputted from pin (40) of IC201, and supplied to pin (1) and (3) of IC2201. Then Y-signal supplied to pin (3), passing through the clamp circuit, is mixed with EE C signal supplied to pin (5) in the IC and outputted from pin (10) via the video amplifier.Y-signal supplied to pin (1), passing through the clamp circuit, is mixed with non-record characters supplied to pin (16) and zone signals supplied to pin (6) in the IC, outputted from pin (15) to become Y-signal for the viewfinder.
The other signal, first passing through the record and playback switch in IC201 for recording, is outputted from pin (61) through LPF and AMP.
Here LPF damps the vicinity of 4.43 MHz in the trap circuit of C212 and L203 of pin (63), and sets the band (– 3dB) at approx. 3 MHz. Then the signal is supplied to pin (60) through C416 then, passing through the clamp circuit, supplied to the non-linear emphasis circuit in the next step, while LP-H signal supplied to pin (6) operates either the detail enhancer circuit or the non-linear emphasis circuit. That is to say that the detail enhancer circuit operates in SP mode and the non-linear emphasis circuit operates in LP mode, obtaining respective characteristics. The signal outputted from these circuits is supplied to the main emphasis circuit.
The characteristics in the main emphasis circuit are determined by R218, R219, and C218.
This circuit applied pre-emphasis, and the white/dark clip circuit clips overshoot components above a specified level (185%) and undershoot components below a specified level (– 45%) and supplied to the FM modulation circuit. Here the signal is modulated into FM signal of 3.8 MHz in the sync chip section and 4.8 MHz in white peak section and outputted from pin (55) of IC201. Further, H-SW-P signal supplied to pin (7) performs FM interleave procesesing in LP mode. The FM-modulated signal is adjusted in record level in R228 and supplied to the FM equalizer circuit. Here the low band components of the FM signal (Record C signal frequency band components) are damped, equalized, then outputted to pin (4) of connector BD-AH.
The signal is supplied to pin (25) of IC301, mixed with low band C signal supplied to pin (27) in another system, then, passing through REC AMP, supplied to the video head via the rotary transformer. Selection of head in recording mode is performed by changing over the switch in IC301 by 4-phase pulse from IC801.

2-3. Flow of playback Y signal

In playback mode, V-REC signal and REC5V are "L" and PB5V is "H", and the rotary transformer and IC301 are in playback mode, and the video head playback a signal from a tape. The playback signal is amplified in the pre-amplifier of PB1-4 and supplied to the selection switch circuit of CH1-4. The switch circuit turns individual playback signal from CH1-4 into a continuous signal, supplies to 10dB PB AMP in the next step, and outputs from pin (41).

The playback signal thus obtained passes through pin (7) of connector AH-BD, is supplied to the buffer of Q410 and divided into two. One is supplied to the playback C signal processing circuit, and the other is supplied either to pin (13) (in SP mode) or to pin (11) (in LP mode) and outputted from pin (16) through the switch in the IC and 12dB AMP.

Then the high band components are amplified and low band conversion C signal is eliminated in the RF equalizer circuit, and the amplitude of FM signal is corrected, then the signal is supplied to pin (17). Then the signal is outputted from pin (3) and pin (7) for phase correction, phase-corrected in R456, L414, and C446, and supplied to pin (2). Next, the signal is outputted from pin (24) after level control is applied in RF AGC circuit.

PM signal thus obtained, whose high band noise components are damped in L403 and C418, is supplied to pin (56) of IC 201. Here the envelope is detected, dropout is detected, and DOC pulse is outputted, as well as the signal is sent to LPF and HPF in the IC to respectively become low band component and high band component supplied to the double limiter.

The signal through HPF is subject to the first step of the double limiter in the next limiter, then it is mixed with said low band components and subject to the second step of the double limiter. The output is demodulated to Y-signal in the demodulator and supplied to the main de-emphasis circuit after FM carrier components are eliminated in sub LPF. The de-emphasis circuit gives the emphasis characteristics in the reverse of those in recording, improves S/N ratio, and supplies the signal to GCA (Gain Control Amplifier) circuit in the next step. Here, after the Y-signal level is adjusted in R415, it is sent to LPF through the record and playback switch. The LPF has completely the same characteristics as in recording, and eliminates residual high band components, then the signal is supplied to the non-linear de-emphasis circuit only in LP mode. In SP mode, the circuit does not operate but the signal is outputted from pin (61).

The Y-signal from pin (61), passing through C416, is inputted in pin (60), clamped, then supplied to the circuit for obtaining a differential signal between the dropout correction switch and 1H delay signal. Here the switch is for changing over with 1H delay signal by DOC signal mentioned above in drop-out mode, and it operates as a video DOC. The Y-signal through the DOC switch is divided into two, one of which is mixed with a signal limiting the differential signal from above-mentioned 1H delay signal as a line correlative noise reduction process. The other is outputted from pin (58) to obtain the 1H delay signal, and supplied to pin (6) of IC403. Here the IC403 is a CCD delay line with a clock of 2fsc (fsc:4.43 MHz), which clock doubles the fsc output from pin (34) of IC201 in IC402, and uses the resultant output. The signal delayed in the CCD delay line is outputted from pin (4) of IC403, passes through the buffer, and delay time of approx. 90 nsec. is added in LPF of L402, C412 and C413 to obtain delay of 1H. Then the 1H delay signal is adjusted in level, supplied to pin (59) of IC201 through AMP and buffer of Q402, clamped, then supplied to the dropout correction switch to become a dropout correction signal.

The Y-signal that has gone through line correlation noise reduction process is then supplied to the video equalizer circuit. The equalizer circuit, which is emitter peaking, corrects the frequency characteristics of the playback Y-signal by a constant of RLC connected to pin (47). The signal is improved in S/N in the noise cancel circuit and supplied to the record and playback switch through the picture quality control circuit.

In EDIT mode set by pin (17), the above line correlation noise reduction operation and picture quality control circuit are turned off, which restrains noise canceling. The playback Y-signal thus obtained, passing through the record and playback switch, is outputted from pin (40) through the sub-clamp circuit and AMP the same as EE Y signal. Then it is supplied to pin (1) and (3) of IC2201, and respectively mixed with playback C signal in pin (7) processed in a system separate from playback Y-signal for the viewfinder, and it becomes the playback video output signal.

2-4. Head amplifier circuit

First, in the record mode, SW1-4 are open, and SW5-8 are on because REC5V is supplied, and the rotary transformer is set in the record mode. When video head R1 (CH1) records a signal on a tape, SW-1 pulse from the system controller circuit is "L", SW9 is opened, and the record signal flows. As other SW-2, SW-3, and SW-4 pulses are "H" during this period, SW10-12 are on, and video heads L1 (CH2), R2 (CH3), and L2(CH4) do not record a signal on a tape. Then L1 (CH2), R2 (CH3), and L2 (CH4) keep on recording in the same manner.
Also when V-REC signal is "L", pin (26) of IC301 becomes "H", and turns on SW9-12, disallowing a record signal to flow in any head and setting REC PAUSE status. This model is equipped with a rotary erase head, which erases a recorded signal in place of the conventional full erase head. In this operation, the ROT ERASE signal from the system controller (IC801) turns on Q3303, and actuates the oscillation circuit consisting of Q3302, Q3301, etc. The oscillation frequency is a resonance frequency of combined capacitance of L3302 and C3304-C3306, approx. 8.8 MHz. Then it is reformed and amplified by C3308 and inductance of the rotary transformer, allowing an erase signal to flow in the rotary erase head.
Then, in the playback mode, PB5V is supplied to the video head turning on SW1-4, and the rotary transformer is set in the playback mode. In playback mode, the above SW1- 4 pulses have their polarity inverted. Therefore when video head R1 (CH1) playback a signal from a tape, SW-1 pulse is "H", then inverted in the inverter to become "L", which open SW5, transmitting a signal from a head to PB1 pre-amplifier.
The output from PB1 pre-amplifier is supplied to SW15 via SW13 transmits the output from PB1 pre-amplifier to SW15 while H-SW-P signal is "H". SW15 outputs the above input when H-AMP-SW signal is "H". The signal outputted from SW15 is supplied to PB5, amplified by 10dB, then outputted from pin (41) of IC301.

Playback output conditions

Output	SW-1	SW-2	SW-3	SW-4	H-SW-P	H-AMP-SW
CH1	H	L	L	L	H	H
CH2	L	H	L	L	H	H
CH3	L	L	H	L	H	L
CH4	L	L	L	H	L	L

2-5. Flow of record C-signal

The C-signal outputted from the camera part is supplied to pin (1) of connector BG. It is first inputted in pin (16) of IC501, the record character part being damped by use of a switch. Then it is outputted from pin (1). The signal is divided into two, one of which becomes EE signal and the other a record signal the same as Y-signal. The EE C signal is level-adjusted in a resistive divider, inputted in pin (5) of IC2201, and supplied to 12dB AMP via the record and playback switch in the IC. The output is mixed with said Y-signal in the IC, outputted from pin (10) through the video amplifier to become EE video output signal.
The record C signal is inputted in pin (3) of IC501, and outputted from pin (12) through the record and playback change-over switch. Then it is inputted in pin (11) of IC201 through 4.43 MHz BPF (FL501), and supplied to ACC AMP through the record and playback switch. Here, FL501 is used for timing with the record Y-signal, whose group delay time is approx. 500 nsec. Then the output from ACC circuit is sent to the main converter circuit, which converts the C-signal of 4.43 MHz into low-band C signal of 627 kHz by the output from sub-converter 5.06 MHz. Here, the output from sub-converter sent to the main converter circuit is balance-modulated by 40.125 fH (627 kHz) divided into 1/8 from VCO (321 fH) and fs (4.43 MHz) from VXO. The output, containing components of sum and difference of 40.125 fH and fs, is outputted from pin (36) of IC201. Then the sum component of 5.06 MHz is taken out by 5.06 MHz BPF (FL502), supplied to pin (18), and sent to the main converter.

The output from the main converter is supplied to LPF through the record and playback switch. The main converter output, whose unnecessary components are eliminated by LPF in the IC, is outputted from pin (22) through the amplifier in the next step. Then it is level-adjusted in R513 and, passing through the buffer, supplied to pin (5) of connector BD-AH. Then it is supplied to pin (27) of IC301, mixed with FM Y signal, and recorded on a tape with high-frequency and high-level FM signal as AC bias.

2-6. Flow of playback C-signal

As described in the flow of playback Y-signal, the components below 100 MHz damped in C513, is supplied to pin (16) of IC201 after passing through the buffer of Q410. Then it is amplified in PB AMP, and supplied to LPF through the record and playback switch. The playback signal, whose unnecessary FM Y signal is damped by LPF in the IC and only low band C-signal taken out, passes through the record and playback switch and ACC AMP, and is supplied to the main converter circuit. The signal of 5.06 MHz is sent to the main converter circuit from the sub-converter circuit the same as in recording, whose output becomes the original C-signal of 4.43 MHz.

The playback signal contains time axis fluctuation (frequency and phase fluctuation) due to tape speed fluctuation, irregular rotation of video head, and tape expansion. Namely, the played back low band conversion burst signal is played back by fsc' = 40.125 fH' ± △ f. Here, fH' represents fH ± △ fH, i.e., frequency fluctuation due to tape speed fluctuation, and SIDE LOCK circuit corrects large fluctuation like 40.125 fH'. On the other hand, fluctuation such as ± △ f due to irregular rotation of video head and tape expansion is corrected by APC loop. Namely, frequency and phase fluctuation is corrected by APC loop usually, while SIDE LOCK circuit operates when frequency fluctuation is beyond correction by APC loop, and pulls it back quickly to the lock range of APC. The SIDE LOCK circuit detects the presence of error signal every 8H, outputs a pulse from pin (29), and corrects APC loop via R521.

These correction signals control 321 fH VCO and oscillate at 321 fH' ± 8 △ f. The output is divided into 1/8 to become 40.125 fH' ± △ f and supplied to ROTARY (PS) circuit. Here, when playback is by CH1 and CH3 head the same as in recording, the phase is advanced by 90 degrees every 1H, and when playback is by CH2 and CH4 head, the phase is delayed by 90 degrees every 1H, and the signal is supplied to the sub-converter.

VXO which oscillated with the phase locked to the input burst signal in record mode is sent to the sub-converter circuit as 4.43 MHz XO in playback mode, and the sub-converter output is (4.43 MHz + 40.125 fH' ± △ f) and (4.43 MHz − 40.125 fH' ± △ f). The sub-converter output, whose (4.43 MHz + 40.125 fH' ± △ f) component is taken out, takes the same route as in record mode, and is sent to the main converter circuit. Therefore, the main converter output becomes the component of sum and difference of playback C signal (40.125 fH' ± △ f) and (4.43 MHz + 40.125 fH' ± △ f) inputted in pin (18).

The output signal from the main converter circuit, passing through the record and playback switch in the IC, is outputted from pin (8), and supplied to 4.43 MHz BPF of FL501. FL501 obtains 4.43 MHz, a differential component between (40.125 fH' ± △ f) and (4.43 MHz + 40.125 fH' ± △ f), namely C-signal with no fluctuation. The playback C-signal thus obtained is inputted in pin (11) of IC201, and outputted from pin (12) after the burst signal recovers the original amplitude in the burst de-emphasis circuit. Then it is supplied to the comb filter DL501, here having the cross talk component of C-signal from the adjacent track eliminated. The comb filter output is inputted to pin (14), and outputted from pin (20) through COMB AMP in the IC, the record and playback switch, and PB AMP.

The playback C-signal thus obtained is level-adjusted in the resistance divider and inputted to pin (7) of IC220. Then it passes through the record and playback switch in the IC, and is mixed with the playback Y-signal by just the same route as EE C-signal to become a playback video output signal.

3. AUDIO CIRCUIT

3-1. Flow of signal

For audio input when VCR is in EE or REC mode, two systems are available, that is a signal inputted from an external MIC terminal and a MIC signal which is machine-electro converted by a microphone.
Also, for input when VCR is in PB mode, there is one system available of PB signal which is magnetic-electro converted by an audio head.
These signals are respectively inputted, adjusted in frequency characteristics and level, and outputted to the audio terminal of AV connector. The flow of such signals is shown in Fig. 3-1.

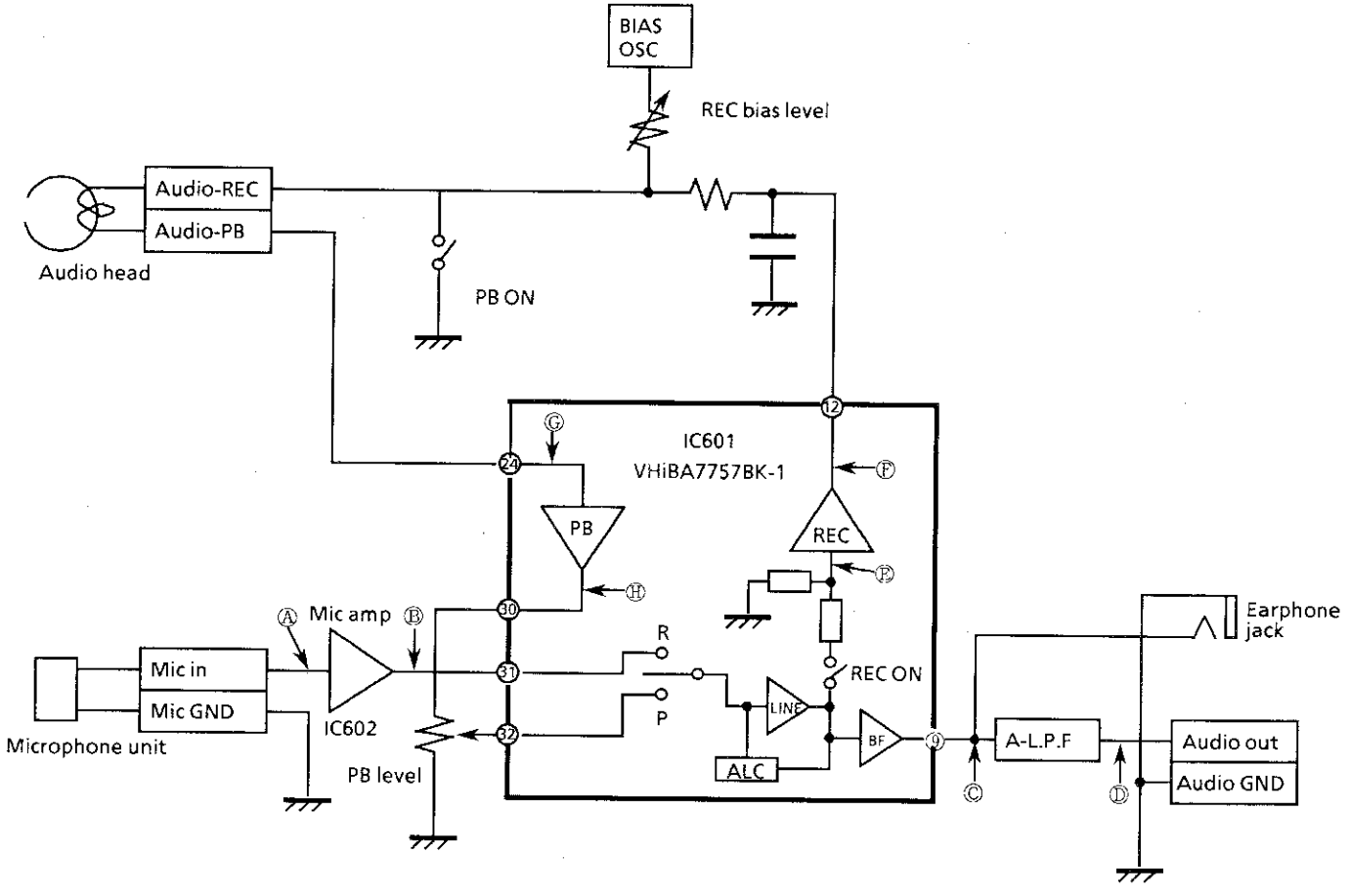


Figure 3-1. Audio Circuit Block Diagram

3-2. Frequency characteristics

1. EE system

General frequency characteristics of external microphone EE system are shown in Fig. 3-2.
In the external microphone EE system, high and low bands are damped by the MIC-Amp (between Ⓐ and Ⓑ in Fig. 3-1) in order to eliminate extra noise, and jump-in of horizontal oscillation frequency 15.625 kHz from the video system is prevented by the LPF (between Ⓒ and Ⓓ in Fig. 3-1).

EE System Frequency Characteristics

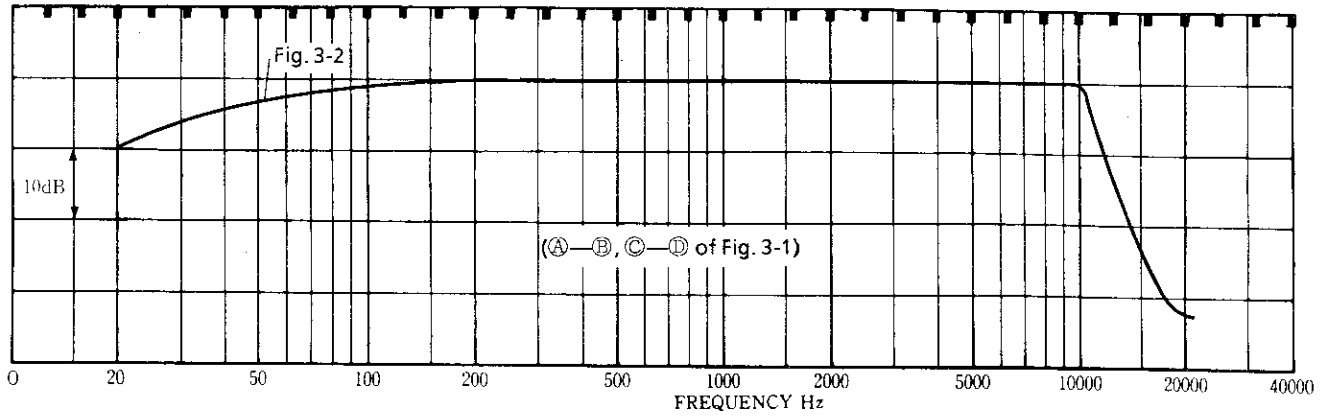


Figure 3-2.

2. REC system

In order to correct the loss in high band due to spacing loss or demagnetization loss, equalization is made by REC-amp (between Ⓔ and Ⓕ in Fig. 3-1) as shown in Fig. 3-3 in SP mode and Fig. 3-4 in EP mode.

REC System Frequency Characteristics

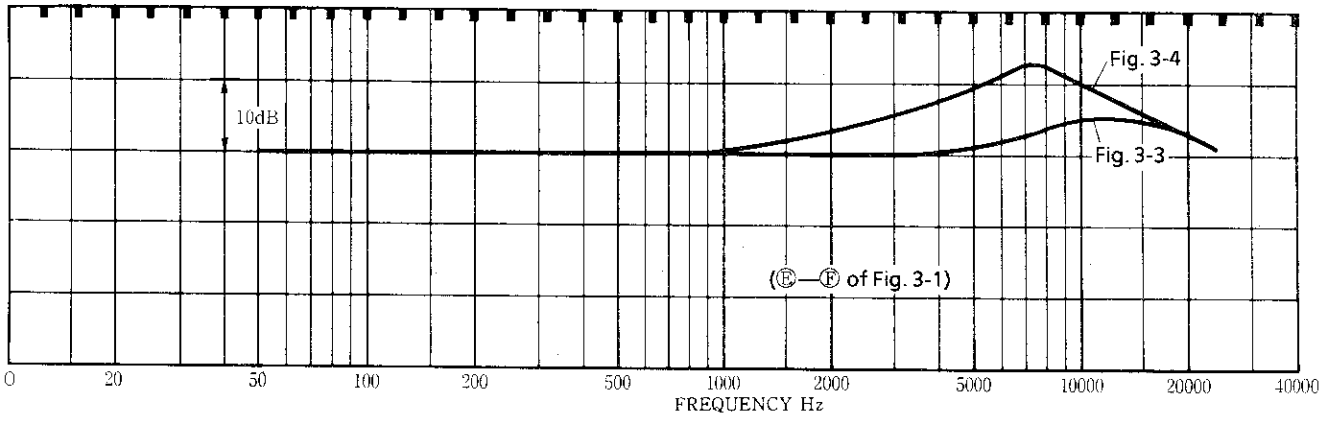


Figure 3-3. and Figure 3-4.

3. PB system

In PB system, equalization is made by the PB-amp (between Ⓖ and Ⓗ in Fig. 3-1) based on VHS standard as shown in Fig. 3-5 in SP mode and Fig. 3-6 in EP mode.

PB System Frequency Characteristics

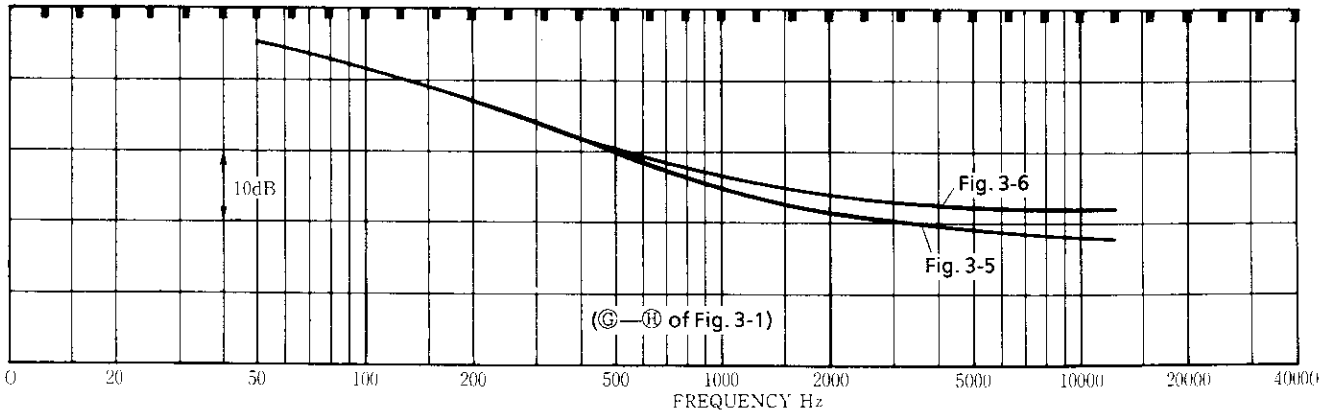


Figure 3-5. and Figure 3-6.

3-3. Signal system and other items

1. Fade

   A linear fade signal inputted from the system control circuit enables audio fade-in and audio fade-out effect nearly synchronized with the video signal. Here, the fade-out effect means an operation where the audio volume, being gradually reduced, finally dies away, and the fade-in effect means an operation where the vanished sound becomes larger and larger until it settles at a certain level.

2. ALC

   ALC, abbreviation for "Automatic Level Control", is an operation where an excess input above a specified level is restrained to the specified level. It is a function to avoid a bad influence such as deterioration of sound quality by saturation of audio head when such excess input can be recorded as it is.

   ALC is programmed to operate at – 8dB by R620 as shown in Fig. 3-7 in this unit.

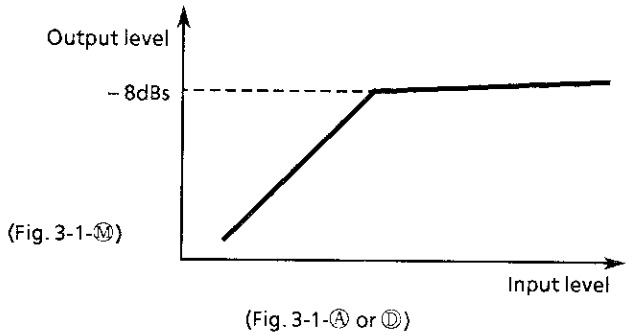


Figure 3-7. ALC Characteristics

3-4. Bias oscillation circuit

The bias oscillation circuit (around T690) oscillates in REC mode, while it does not in other modes. The oscillation frequency is 70 kHz.

4. POWER CIRCUIT

4-1. Outline

Switching regulator system is adopted in order to make the unit compact, light, and efficient. The output voltage is 5V, 9V, 17V, and – 13V, and Capstan Motor power source (PWM output) and Drum Motor power source (PWM output) are available. The circuits to which battery voltage 9.6V is directly inputted are system controller circuit (system controller 50 Reg), loading motor power source, and camera part (such as a zoom motor). In addition, 8.5V series regulator is available as a sensor power source.

4-2. Description of circuit

1. TL1451 ACNS (IC901)

1) See block diagram 4-1.

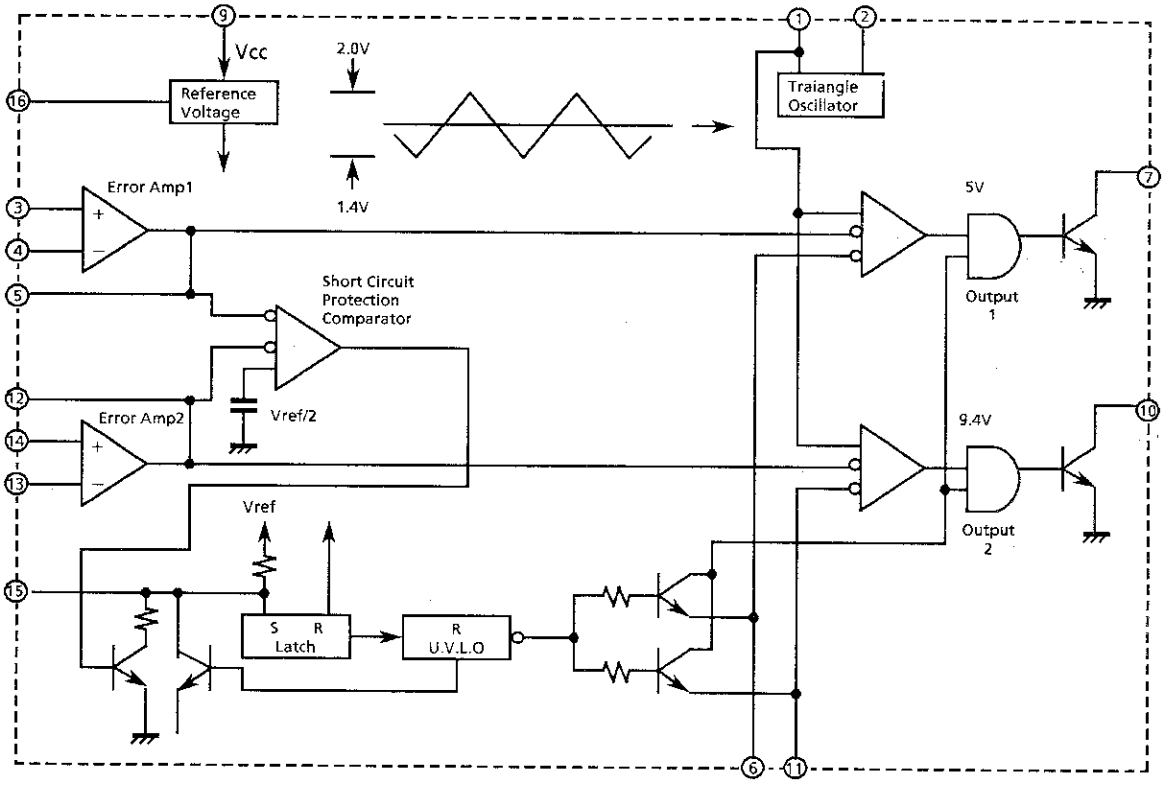


Figure 4-1. Block Diagram of TL1451

2) Description of function

(a) Reference voltage part

P-con 9.6V (9 – 11.5V) applied by the Vcc (pin (9)) terminal composes a temperature-compensated reference voltage power source of 2.5V, which is used as an operation power source for the analogue circuit within the IC. It is also taken out through the Vref (pin (16)) terminal, creating 1.25V in the resistance divider, which is used as a reference voltage of the comparator.

(b) Chopping wave oscillator

The timing capacitor (180P) and resistance (18 kohms) are connected to the C_T (pin (1)) terminal and R_T (pin (2)) terminal to generate a chopping wave oscillation waveform of approx. 200 kHz, whose voltage amplification is between 1.4 and 2.0V.

The waveform is connected to the non-inversion input of PWM comparator in the IC as well as taken out through the C_T (pin (1)) terminal, and connected to the non-inversion input (pin (3) and (5)) of IC902 (NJM2403M) for drum PWM and capstan PWM circuits.

(c) Error amplifier

The error amplifier is a circuit to detect the output voltage of 5V and 9V regulator circuit. Equal-phase input voltage of the error amplifier ranges from 1.05V to 1.45V, and reference voltage output is divided by resistance and connected to respective inversion input terminal (pin (4) and pin (13)). The output (pin (5) and pin (12)) terminal of the error amplifier connects a capacitor and resistance to respective inversion input terminal, applying feedback. Also the output of the error amplifier is connected to the inversion input of PWM comparator as well as to the detection circuit of the incorporated short-circuit protective circuit.

(d) Timer-latch system short-circuit protective circuit

The circuit is a comparator having two inversion inputs and a non-inversion input, and when either or both of error amplifier to detect an output level of respective error amplifier output less than Vref/2, it outputs "HIGH" level, triggers the timer circuit, and the externally installed (pin (15)) protection enabling capacitor C954 starts charging. When the output of the error amplifier does not recover a normal voltage range before the capacitor voltage reaches V_{BE} (approx. 0.6V) of the transistor, it sets the latch circuit, and disables the output drive transistor as well as sets the rest period at 100%.

(e) Low input malfunction prevention circuit

In a momentary drop of power source line due to transient condition in power-on and unexpected accident, it detects the incorporated reference voltage level and resets the latch circuit in accordance with the power source voltage level thereby disabling the output drive transistor, and sets the rest period at 100% as well as keeps the protection enabling terminal "LOW".

(f) PWM comparator

The PWM comparator has two inversion inputs and non-inversion input respectively. It is a voltage pulse width converter which controls "ON" time of the output pulse in accordance with the input voltage using a voltage comparator.

It turns on the output drive transistor in the period when the chopping wave from the oscillator is higher than both of the dead time control terminal voltage (pin (6) and pin (11)) and malfuction amplifier output.

The dead time control terminal for 5V Reg (pin (6)) is connected to GND, comparing only the error amplifier output and chopping wave. Approx. 1.6V is inputted to the dead time control terminal (pin (11)) for 9V Reg by dividing the reference voltage Vref with a resistance, preventing the output drive transistor from remaining "ON" in set-up of the power source.

(g) Output drive transistor

The output drive transistor is outputted by the common emitter single-end open collector and drives the switching power transistor.

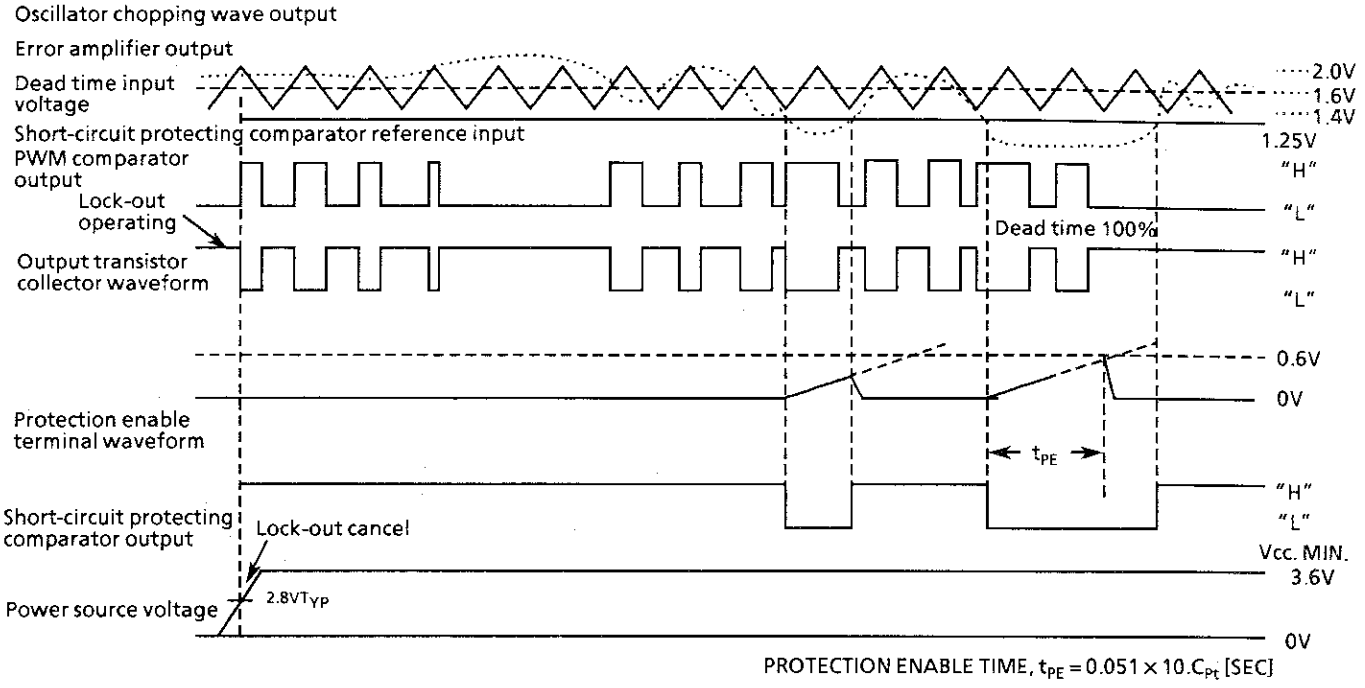


Figure 4-2. TL1451 Timing Chart

2. 5V regulator circuit

   The parts used as a switching regulator circuit are the switching transistor Q920 (2SB956), diode D920 (SFPB64), smoothing coil L930 (100µH), and capacitor C950 (120µF, 6.3V). The pulse width of Q920 output of the circuit is fluctuated by IC901, thus controlling the voltage. Q921 (FMY1) is for driving Q920.

   The 5V output is suppplied to the VCR circuit (V/F circuit) and camera circuit, switched by Q960 (2SD1757) to the camera circuit.

3. 9V regulator circuit (17V, 11.5V, and – 13V output)

   The multi-pulse transformer T901 is switched by Q940 (2SA1213), and it outputs 17V, 11.5V, 9V, and – 13V. The 9V output is fed back to IC901, fluctuating the pulse width of Q940 output and controlling the voltage. Q941 is for driving Q940. D921, D914, D940, D923, C945, C930, C943, and C948 are for rectification of each output. The 9V output is supplied to the VCR circuit and camera circuit, switched by Q933 (2SA1577) to the camera circuit. Also the 17V and – 13V outputs are switched by Q931 and Q930.

CAMERA SECTION

5. CAMERA MICROCOMPUTER CIRCUIT

Camera microcomputer IC655 performs input of each operation keys, execution of each camera functions, data transfer with the VCR microcomputer and waveform adjustment of the signal processing circuit.

5-1. Outline of function

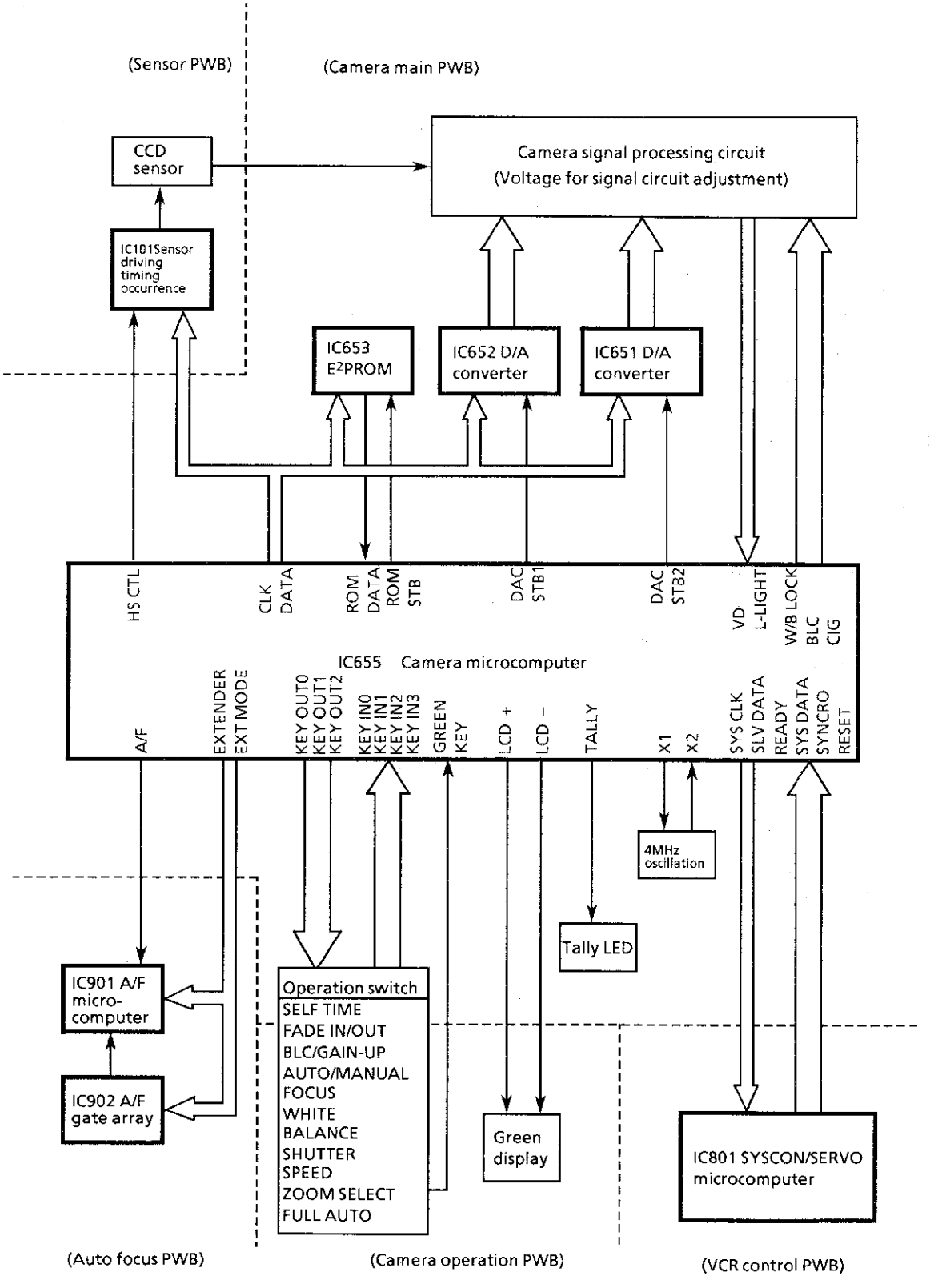
1. Key input
   1) Matrix key input
      - Auto/Manual focus
      - White balance
      - Shutter speed
      - BLC/Gain-up
      - Zoom select
      - Self timer
      - Fade-in/Fade-out
   2) Other keys input
      - Full auto
      - Pause remote

2. Camera function control
   1) Focus ——— Auto/Manual switching
   2) Shutter speed ——— Speed switching
   3) White balance ——— Auto/Lock switching
   4) BLC ——— ON/OFF
   5) Gain-up ——— ON/OFF
   6) Zoom select ——— Standard/Zoom (1.5 times) switching

3. Display control
   1) Talent tally LED display
   2) Full auto LCD display

4. Serial transfer
   1) Master controller (VCR microcomputer)
   2) E^2PROM
   3) D/A converter ——— (signal processing circuit adjustment)

5-2. Camera microcomputer peripheral block



5-3. Terminal configuration

Z: HIGH impedance

pin	name	LABEL NAME	IO	FUNCTION	TERMINAL TYPE	REMARK
1	P41	EEPROM IN	I	EEPROM SERIAL DATA INPUT		
2	P40	SH MODE	I	SHUTTER MODE SELECTION		
3	P53	CIG SEL	I	CIG OUTPUT MODE SELECTION		
4	P52					
5	P51	LO LIGHT	I	H INPUT AT LOW ILLUMINANCE		
6	P50					
7	RESET	RESET	I	RESET		
8 9	X2 X1			4MHz OSCILLATION		
10	P63	A/F	O	H OUTPUT AT AUTO FOCUS	C MOS	
11	P62	MOVIE LIGH	O	H OUTPUT AT MOVIE LIGHT	C MOS	NOT USED
12	P61	CIG	O	H OUTPUT AT LOW ILLUMINANCE GAIN CONTROL	C MOS	
13	P60	WB LOCK	O	H OUTPUT AT WHITE BALANCE LOCK	C MOS	
14	P73	EXTENDER	O	H OUTPUT AT EXTENDER	C MOS	
15	P72	BLC	O	H OUTPUT AT BACK-LIGHT CORRECTION	C MOS	
16 17	P71 P70	LCD 1 LCD 2	O O	LIQUID CRYSTAL DRIVE SIGNAL 1	C MOS	
18 19 20 21 22 23 24	P83 P82 P81 P80 P93 P92 P91	SIP R SIP G SIP B SIP ON/OFF SIP INV SIP ME ME	O O O O O O O	SUPERIMPOSE R SIGNAL SUPERIMPOSE G SIGNAL SUPERIMPOSE B SIGNAL SUPERIMPOSE ON-OFF SIGNAL SUPERIMPOSE REVERSE SIGNAL	C MOS	NOT USED NOT USED NOT USED NOT USED NOT USED NOT USED NOT USED
25	P90	EFFECT CTL	O	EFFECT CONTROL SIGNAL	C MOS	NOT USED
26	Vss					
27 28	INT3 INT2					
29	INT1	VD	I	TEST MODE AT L INPUT		
30	INT0	RC KEY	I	REMOCON INPUT		
31	PTHO3	REC S/S	I	REC S/S INPUT (FF40 CORRESPONDENCE)		NOT USED
32 33 34	PTHO2 PTHO1 PTHO0					
35 36	T10 T11					
37	P23	EXTmodeCTL	O	H OUTPUT AT EXTENDER		
38 39 40	P22 P21 P20	SMD 2 SMD 1 SMD 0	O O O	HIGH SPEED ELECTRONIC SHUTTER	C MOS	NOT USED
41 42 43 44	S1 S0 SCK INT4	MDATA CDATA CLK READY	I O O I	SERIAL TRANSFER DATA INPUT SERIAL TRANSFER DATA OUTPUT SERIAL TRANSFER CLOCK SERIAL TRANSFER TRANSFER DEMAND	C MOS C MOS	
45 46	P123 P122	DATA CLK	O O	PERIPHERAL SERIAL CONTROL COMMON DATA PERIPHERAL SERIAL CONTROL COMMON CLOCK	N ch OD	

pin	name	LABEL NAME	IO	FUNCTION	TERMINAL TYPE	REMARK
47	P121	EEPROM CS	O	SERIAL EEPROM SELECTION	N ch OD	
48	P120	HS CTL	O	SERIAL ELECTRONIC SHUTTER CONTROL	N ch OD	
49	P133	DAC STB 3	O	3	N ch OD	NOT USED
50	P132	DAC STB 2	O	SERIAL DAC STROBING 2		
51	P131	DAC STB 1	O	1		
52	P130	TALLY	O	L OUTPUT AT TALLY DISPLAY	N ch OD	
53	P143	KEY OUT 3	O	KEY MATRIX OUTPUT	N ch OD	
54	P142	KEY OUT 2	O			
55	P141	KEY OUT 1	O			
56	P140	KEY OUT 0	O			
57	NC					
58	Vdd					
59	P33	KEY IN 3	I	KEY MATRIX INPUT		
60	P32	KEY IN 2	I			
61	P31	KEY IN 1	I			
62	P30	KEY IN 0	I			
63	P43	GREEN	I	GREEN CLOCK		
64	P42					

5-4. Matrix key input and output action

The camera microcomputer discriminates the keys being pressed by means of the key scan (active LOW). In case of multiple key pressing (except BLC), key input is kept invalid until all the pressed keys are made unpressed.

When a key is pressed with BLC being pressed, the key other than BLC is made valid. In case of triple key pressing, key input is kept invalid until the pressed keys other than BLC or all the pressed keys are made unpressed.

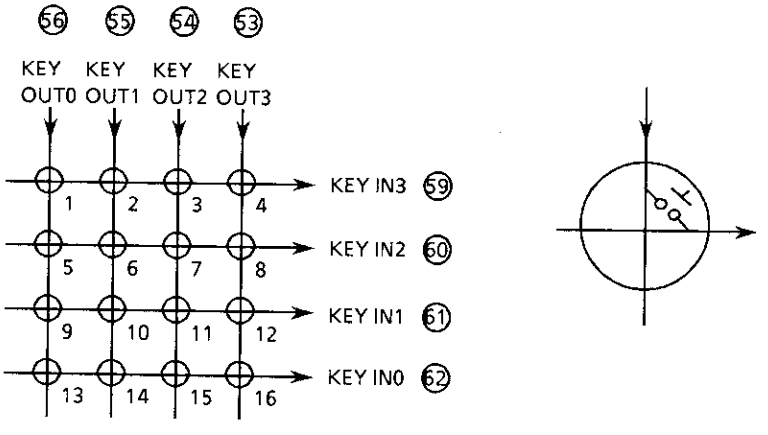


Figure 5-4 (a). Matrix Key Input Circuit

1	FADER	2	REC REVIEW *	3	EFFECT *	4	
5	SELF TIMER	6	SHUTTER	7	SIP MEMO *	8	
9	EXTENDER	10	W/B LOCK	11	SIP COLOUR	12	
13	BLC	14	AF	15	SIP *	16	

Table 5-4 (a). Matrix Key Table * Not used

1. Shutter speed

Each time the operation switch (SW007) is pressed, the shutter speed is switched in order of 1/10000, 1/2000, 1/500, 1/100 and standard.

The camera microcomputer output shown in Table 5-4 (b) and Fig. 5-4 (b) is inputted in the sensor timing IC (IC101) to switch the CCD sensor driving.

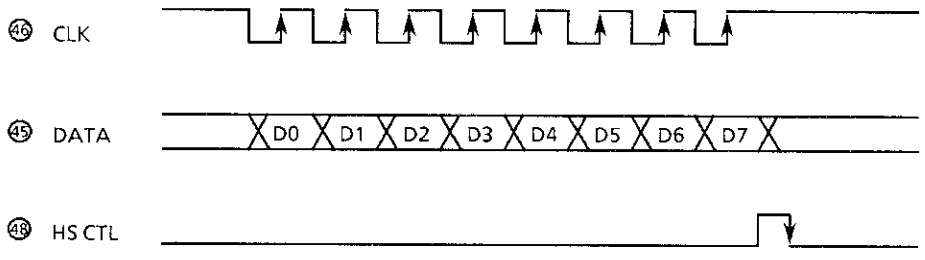


Figure. 5-4 (b). Serial Transfer Waveform

Times of SW ON		1	2	3	4
Shutter speed	Standard	1/10000	1/2000	1/500	1/100
D0	L	H	H	H	L
D1	L	H	L	H	L
D2	L	H	H	L	L
D3	H	H	H	H	L
D4	H	H	H	H	H
D5	L	H	H	H	H

D6, D7: Don't Care

Table 5-4 (b). Data Configuration of Fig.5-4 (b)

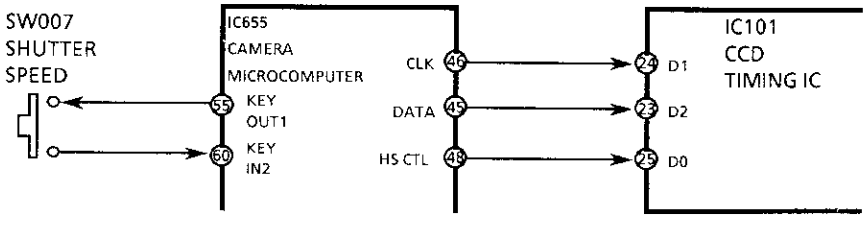


Figure. 5-4 (c).

2. White balance

Each time the operation switch (SW006) is pressed, the camera microcomputer output (13) W/B LOCK is switched to "H" or "L". When the output is "H", output "L" reversed at Q652 is applied on the base of Q301, raising to +5V line the W/B control IC (IC301) input (25) B-Y AWB START and (27) R-Y AWB START terminals respectively, by which the white balance is locked.

SW006	⑬ output	White balance
Once ON	H	Lock
Twice PM	L	Auto

Table 5-4 (c).

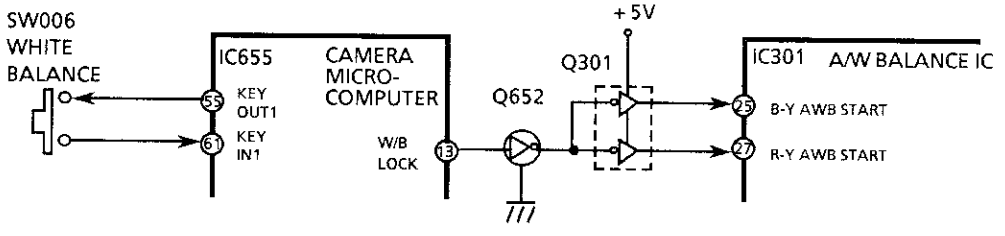


Figure 5-4 (d).

3. Auto/manual focus

Each time the operation switch (SW005) is pressed, the camera microcomputer output (10) A/F microcomputer "L". The output is received by the A/F microcomputer (IC901), switching the focus action to AUTO or MANUAL.

SW006	⑩ output	Focus
Once ON	L	Manual
Twice ON	H	Auto

Table 5-4 (d).

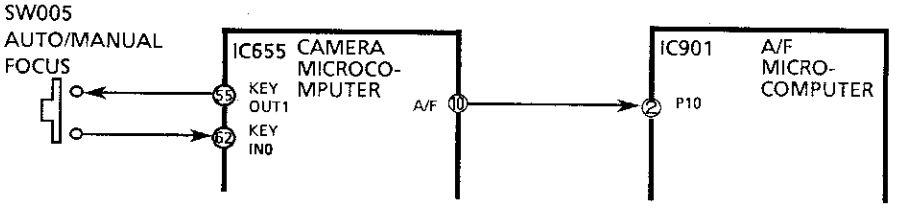


Figure 5-4 (e).

4. BLC/gain-up

When the operation switch (SW003) is pressed, the camera microcomputer output (15) BLC is s
"H". When the output is "H", Q804 reduces the amp gain of the Y/C signal and AGC-Y signal of th
and ALC amp (IC803) respectively.

The iris circuit opens the iris so that the reduction of the Y/C signal is compensated; the gain of the AGC circuit is increased so that the reduction of AGC-Y signal is compensated, back-light correction being performed.

When the camera microcomputer input (5) L-LIGHT is "H" (at low illuminance), each time the operation switch (SW003) is pressed, the camera microcomputer output (12) CIG is switched to "H" or "L". When the output is "H", the signal processing IC (IC201) gets the internal +6dB amp operating, gain-up being performed.

SW003	⑤ input	⑮ output	BLC	output	Gain-up
ON	L	H	ON	L	OFF
OFF	L	L	OFF	L	OFF
Once ON	H	L	OFF	H	ON
Twice ON	H	L	OFF	L	OFF

Table 5-4 (e).

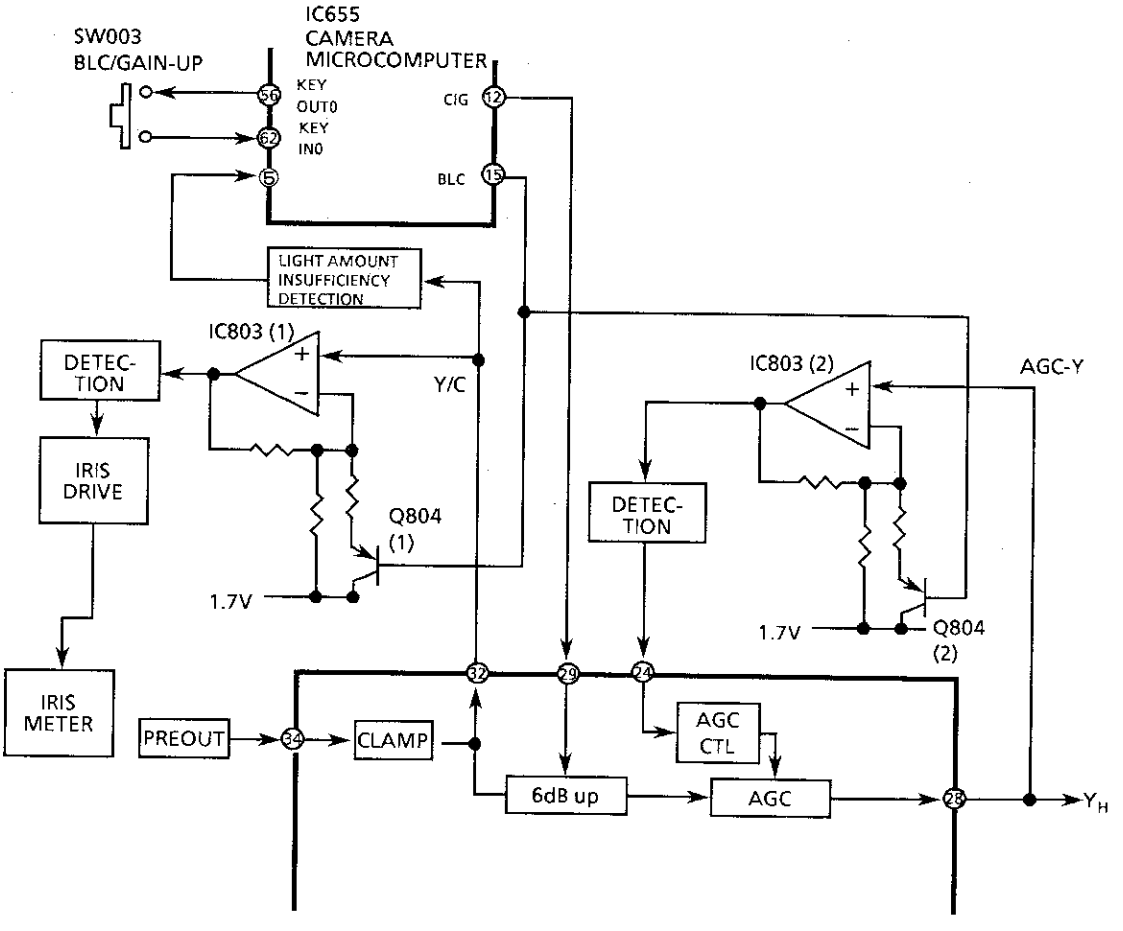


Figure 5-4 (f).

witched to AGC

n switch (SW002) is turned ON, the camera microcomputer output (14) EXTENDER is
". The A/F microcomputer (IC901) detects the change of output signal and switch the
"standard" accordingly.
utput, the A/F gate array (IC902) outputs the EXT GATE signal (enlarged area display
s the viewfinder display.

SW002	⑭ output	Lens	Viewfinder display
Once ON	(H)	1.5 times	Absent
Twice ON	(L)	Standard	Present

Table 5-4 (f).

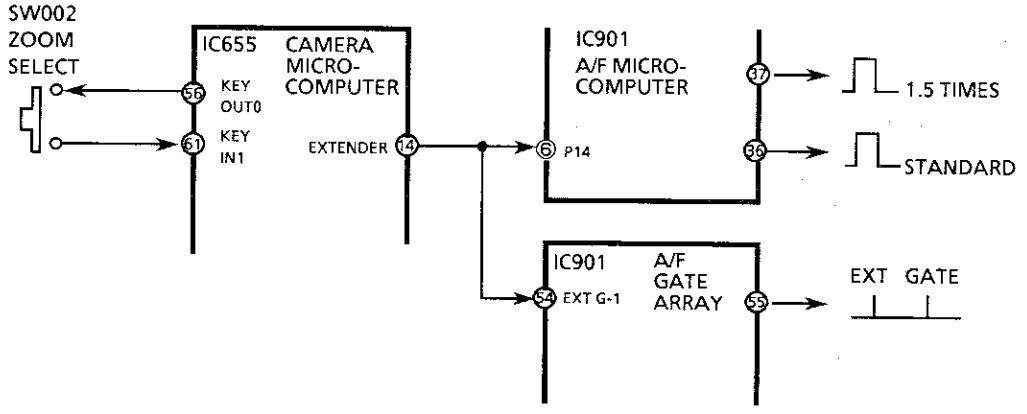


Figure 5-4 (g).

5-5. Other keys input and output action

1. Full auto key

When the FULL AUTO switch (SW001) is switched to "FULL AUTO", the camera microcomputer input (63) GREEN KEY terminal becomes "H" input, setting the camera microcomputer output (10) A/F, (13) W/B LOCK and (45) DATA in the fixed mode.

SW001	Focus, White balance, Electronic shutter, Key input	⑩ output (focus)	⑬ output (white balance)	㊺ output (shutter)
H	Unallowed	H (auto)	L (auto)	Standard data (standard)
L	Allowed	Changes according to the input		

Table 5-5 (a).

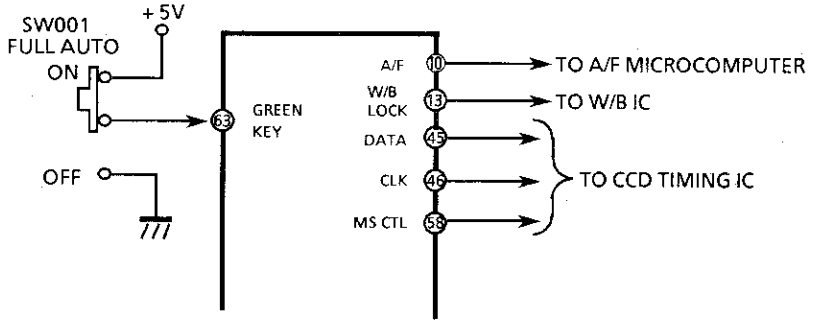


Figure 5-5 (a).

2. Pause remote

The input signal of the REMOTE JACK (J8803) of the VCR operation section is inputted in the camera microcomputer input (30) PAUSE REMOTE.

The camera microcomputer transfers the input signal of the pause remote control connected to the terminal to the VCR microcomputer.

Condition of remote jack	㉚ input
Open (Pause remote control switch OFF)	H
Pause remote control switch ON	L

Table 5-5 (b).

5-6. Other output action

1. Lighting of talent tally LED

At starting REC, according to the data sent from the VCR microcomputer, the LED (D501) is lit by means of the camera microcomputer output (52) TALLY terminal.

⑫ output	D501
H	Putting out
L	Lighting

Table 5-6 (a).

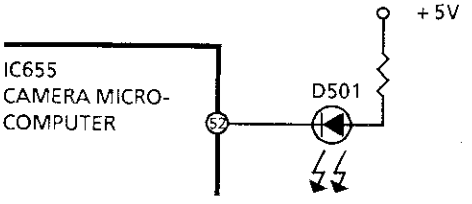


Figure 5-6 (a).

2. Lighting of full auto LCD

According to the state of camera micrcocomputer input (63) GREEN KEY set by the green lock switch (SW001) and the data sent from the VCR microcomputer, the LCD is driven by means of the camera microcomputer output (16) LCD + and (17) LCD −.

⑬ input	VCR microcomputer data	⑯ and ⑰ output	LCD
H	With tape capable of recording	Continuous	Lighting
H	Without tape capable of recording	Intermittent	Flashing
L	Without tape capable of recording	Intermittent	Flashing

Table 5-6 (b).

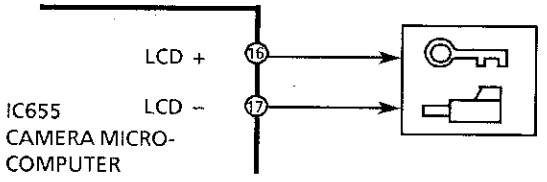


Figure 5-6 (b).

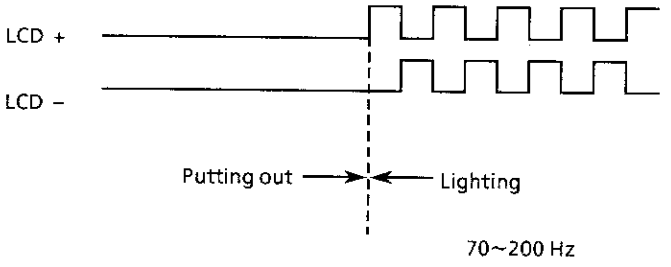


Figure 5-6 (c).

5-7. Camera signal adjustment

The camera microcomputer sends the data written in the E²PROM (IC653) to the two D/A converters (IC651, IC652) and holds the 12 items of waveform adjustment sate in the signal processing process by means of the D/A converter output voltage.

Adjustment mode

The camera microcomputer is switched to the adjustment mode by means of the serial transfer data from the VCR microcomputer. In the adjustment mode, the key scan is stopped, accepting no camera operation keys. Adjustment is made with the VCR operation keys.

Note: For more datails, see the Service Manual "ADJUSTING METHOD OF CAMERA SECTION".

5-8. Serial transfer with VCR microcomputer

The camera microcomputer performs sending/receiving of the serial data with the VCR microcomputer for discrimination of action mode, viewfinder display of operation state, camera function backup, etc.

Transmission function	Action of camera microcomputer	Direction of transmission	Action of VCR microcomputer
	SW input, AUTO/LOCK switching	→	Viewfinder display
CIG	SW input, GAIN-UP/NORMAL	→	Viewfinder display
A/F	SW input, AUTO/MANUAL	↔	Viewfinder display, Backup
EXTENDER	SW input, 1.5 TIMES/STANDARD	↔	Backup
SHUTTER	SW input, Speed switching	→	Viewfinder display
L-LIGHT	Input at low illuminance	→	Viewfinder display
FADE	SW input	→	Viewfinder display, FADE IN/OUT
GREEN	Auto lock ON/OFF, LCD lighting control	↔	Data state input
REMOCON	Remote control input	→	REC start/stop
SELF TIMER	SW input	→	Timer REC (1) and (2)
EE	Camera function acceptance is allowable.	←	Camera mode
TALLY	LED lighting	←	REC RUN mode
PROGRAM	Shifting to adjustment mode	←	Camera adjustment mode
DA OUT	Alteration of address data and adjustment data	←	Adjustment key input
WRITE	Writing adjustment data in ROM	←	Adjustment key input

Table 5-8. Main Transmission Contents

6. WHITE BALANCE CIRCUIT

6-1. Outline

In the white balance section, the video signal processing method is adopted eliminating the conventional white balance sensor exposed outside. Adjustments are all made automatically and the white balance adjusting data of the indoor/outdoor auto offeset are stored in the E^2PROM.
The principle of action is described below.

6-2. Description of action

When white balance is kept under a light source of 3200°K and white is imaged, the colour difference signal output pin (12) and pin (15) of IC201 becomes zero (Fig. 6-2 (a)).
When white is imaged outdoors in this condition, the B-Y colour difference signal pin (12) changes into the signal with amplitude in the positive direction from the blanking section; the R-Y colour difference component into the signal with amplitude in the negative direction (Fig. 6-2 (b)). Consequently, white becomes cyan colour.
On the contrary, when white is imaged under a light source of 3200 K after keeping white balance outdoors (Fig. 6-2 (c)), pin (12) changes into the signal with amplitude in the negative direction from the blanking section; pin (15) into the signal with amplitude in the positive direction (Fig. 6-2 (d)).
In the signal processing white balance circuit, the changed amount of the colour difference signal corresponding to the change of colour temperature is detected and the white balance setting terminal of IC201 is controlled so that the level of the colour difference signal becomes zero.
The system block diagram is shown in Fig. 6-2 (e).

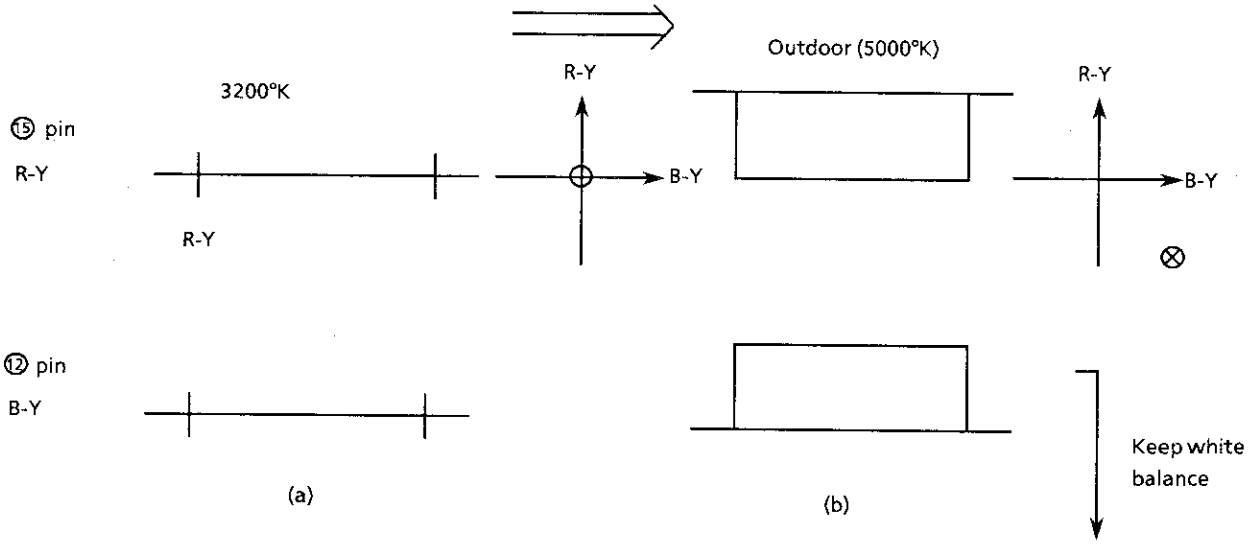


Figure 6-1. Influence of Colour Temperature on Colour Difference Signal in Fixed White Balance

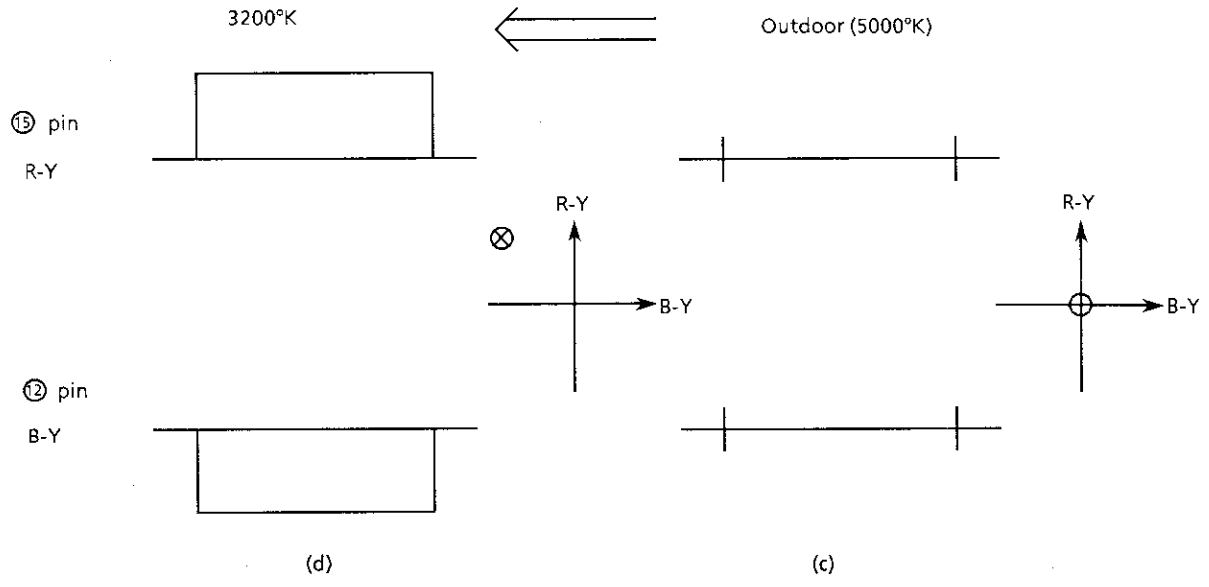


Figure 6-1. Influence of Colour Temperature on Colour Difference Signal in Fixed White Balance

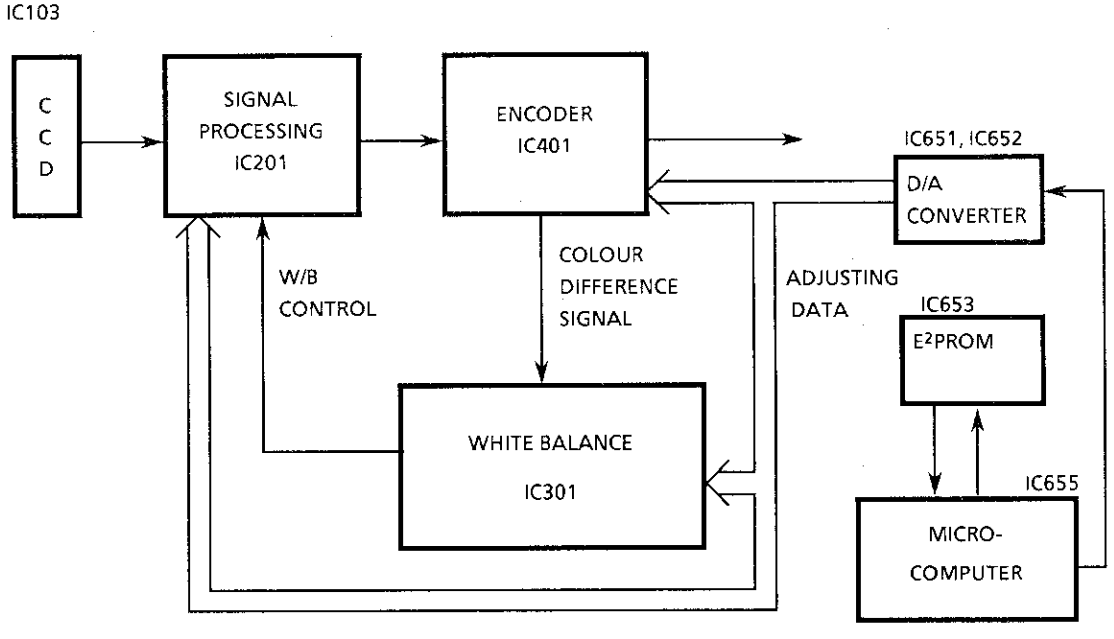


Figure 6-2 (e). System Block Diagram

1. Colour temperature detection

   The signal processing white balance detects the colour temperature with the colour difference signal and performs white balance correction. The colour difference signal having experienced carrier balance at encoder IC401 is at-tenuated at R322, R323, R325 and R326, sent to pin (24) and pin (4) of IC301 through the buffer of Q302, and then subject to clamping combinationat capacitors C303 and C309.

   After being clamped to 1/2 Vcc in IC301, the colour difference signal part in the colour temperature detection area shown in Fig. 6-2 (f) is extracted.

When the following are set,

B-Y/H pin (23) potential
B-Y/L pin (21) potential
R-Y/H pin (5) potential
R-Y/L pin (7) potential

IC301

the shaded portion shown in Fig. 6-2 (f) is set as a detection area set by means of the internal logic. This area is in accordance with the colour temperature colour change characteristics, by which white balancew correction is performed.

The colour difference of the extracted colour temperature colour component is averaged by detection capacitors C305 and C311 of pin (20) (B-Y) and pin (8) (R-Y) and compared with the white balance start setting potential pin (25) and pin (27). If it is lower than the white balance start setting potential, white balance correction action is not performed. This is for preventing the fading caused when an object with low chroma is imaged in the colour temperature detection area and white balance correction is performed.

The white balance lock raises the start setting potential pin (25) and pin (27) to "H" by means of Q301. As the colour difference average of the colour temperature and colour component dose not exceed the start setting potential, white balance correction is not performed.

In addition to the colour temperature detection area shown in Fig. 6-2 (f), the fluorescence detection area shown in Fig. 6-2 (g) is provided. If fluorescence is image after keeping white balance in daylight, it looks yellowish. As this is not covered by the area shown in Fig. 6-2 (f), the fluorescence detection area is provided.

In this area, R-Y is set to the internal fixation; B-Y is set to the V_{Ref} + F.SET by means of pin (26) potential.

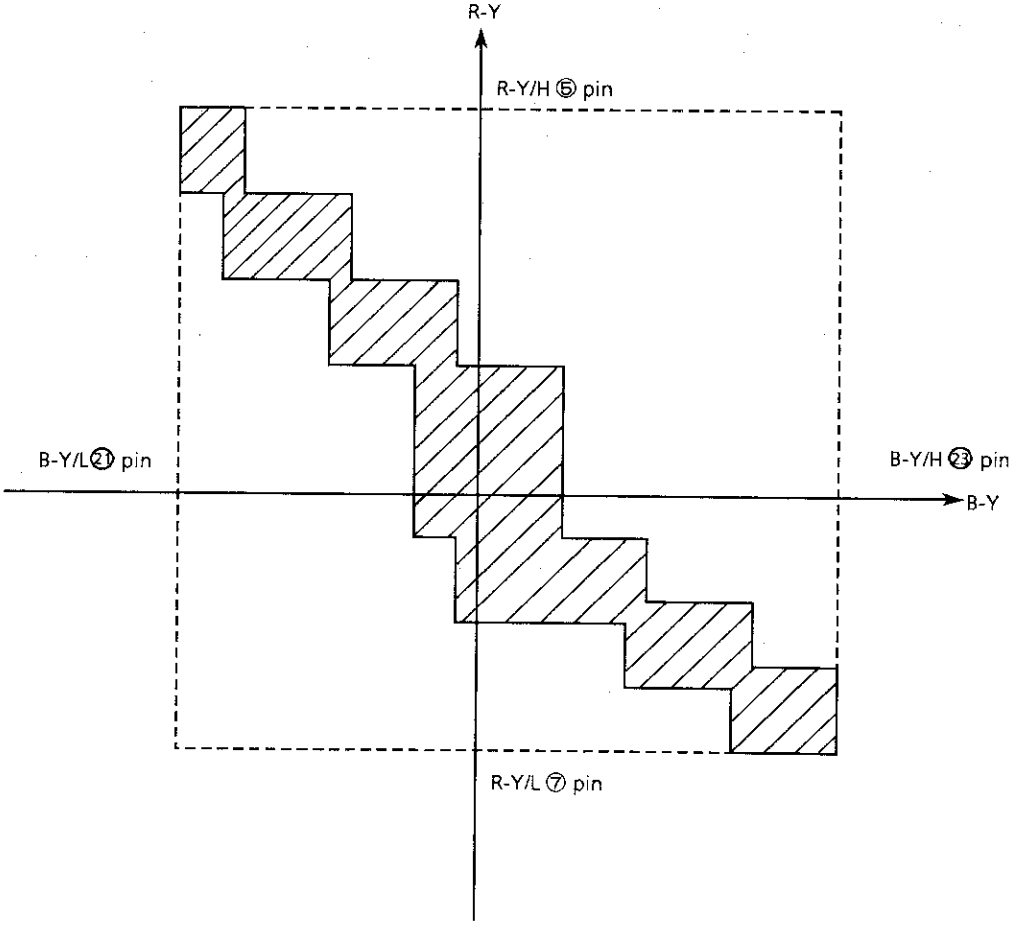


Figure 6-2 (f). Colour Temperature Colour Detection Area

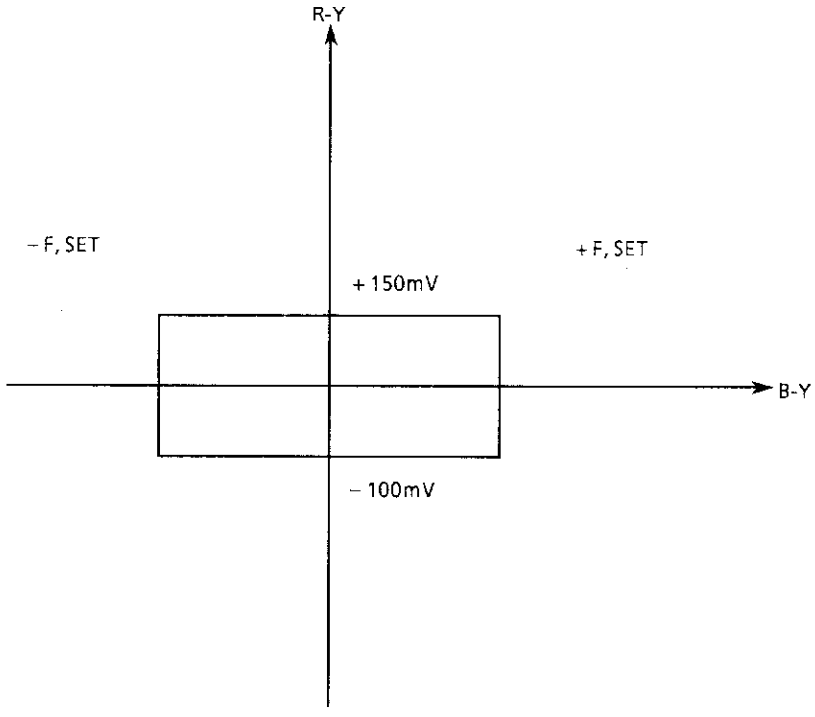


Figure 6-2 (g). Fluorescence Detection Area

2. White balance control section

White balance correction is controlled by means of the preset potential given from the outside. Each preset value of R-Y and B-Y is given as follows:

PRESET		B-Y	R-Y
H	High colour temperature	pin (17)	pin (13)
M	Reference colour temperature	pin (18)	pin (12)
L	Low colour temperature	pin (19)	pin (11)

As shown in Fig. 6-2 (h), the internal preset reference values are set by dividing the portion between M and H into seven in the inside.

There are eight sets of internal preset values corresponding to the internal preset reference values. The white balance control voltage becomes the integral of the time division signal of the internal preset values. For example, when the white balance control voltage is between H4 dand H5, PR5 is selected and the white balance control voltage becomes the integral of the time division signal of the values h and l of PR5.

When the white balance is kept at a certain colour temperature, a set of internal preset values (Fig. 6-2 (h)) is selected and the duty is set so that the optimum white balance control voltage is provided to make the colour difference average get nearest to the white level.

If the colour temperature changes, the duty also changes to perform white balance correction. However, the range of colour temperature change is limited according to which white balance correction can be performed by the duty change within a set of internal preset values. Therefore, when the colour temperature changes greatly, value h or l is constantly outputted without being able to perform white balance correction. Shifting to the next internal preset value is performed by comparing the white balance voltage with the internal preset reference value. The shifting is made only when the colour average exceeds the start setting value.

Pin (10) is the terminal for initialization. When the power is turned ON, it initializes the white balance control output of M preset value (3200°K) by means of R338, R337 and C312. When the power is turned OFF by D302, it rapidly discharges the charged voltage.

C-BLK is inputted in pin (9) EXT SCTL to cut the signal in the image blanking portion.

ENCP pulse is inputted in pin (2) to use as an internal clamp pulse and clock.

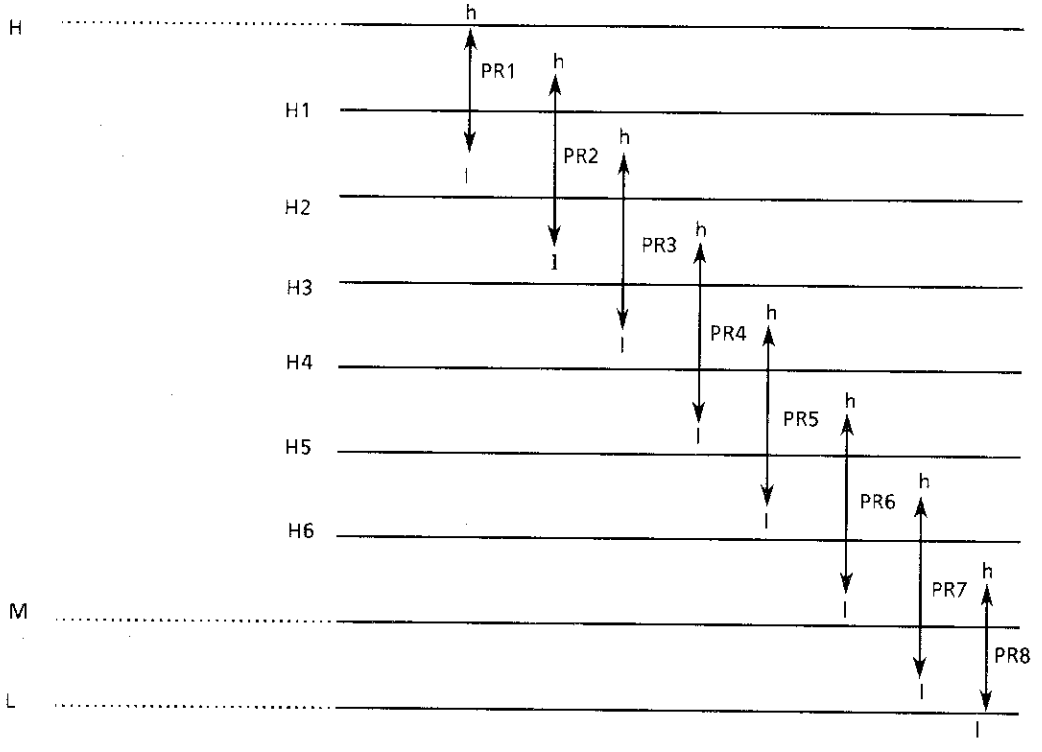


Figure 6-2 (h). Preset Reference Value Setting

3. One axis correction

Diode D301 and resistor R343 are added between pin (15) and pin (14) to control one axis correction, which limits the white balance control range to the vicinity of I axis.

The state with no one axis correction (see Fig. 6-2 (i))

For example, white is imaged in a light source of 3200°K.

At this time, the following equation is obtained.

Pin (15) voltage : V_{B0} = Pin (14) voltage : V_{R0}

= V_{Ref}

Then, colour signal A on B-Y axis in the detection area is imaged. As white balance correction is performed by means of colour signal A, the following equations are obtained.

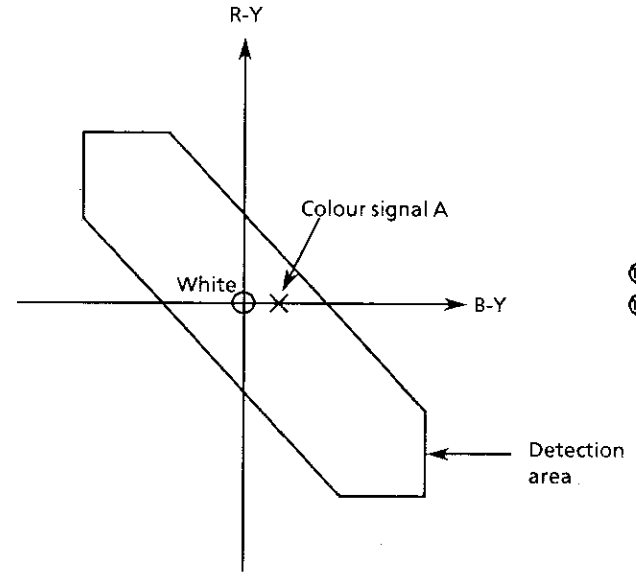
$V_{B1} = V_{B0} + \alpha$ $V_{R1} = V_{R0} = V_{Ref}$

White shifts on - (B-Y) axis by A.

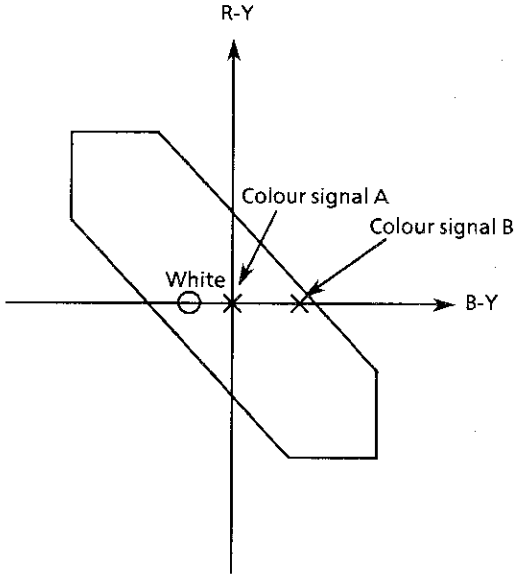
In the same way, colour signal A on B-Y axis in the detection area is imaged. The control potential is expressed as follows:

$V_{R2} = V_{B1} + \beta = V_{B0} + \alpha + \beta$

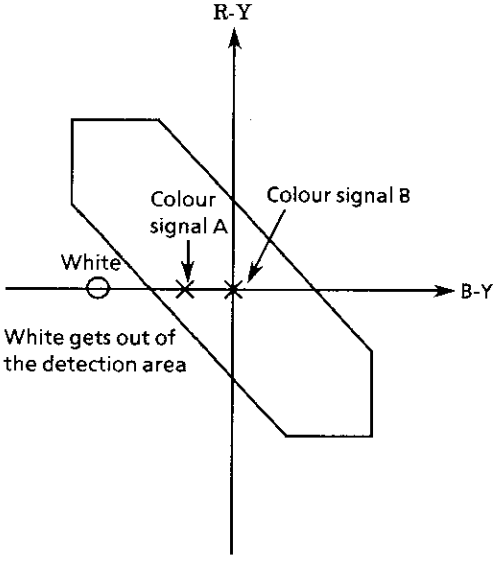
$V_{R2} = V_{R1} = V_{R0} = V_{Ref}$



Lighting source of 3200°K
Imaging of white
⑮ pin potential $V_{B0} = V_{Ref}$
⑭ pin potential $V_{R0} = V_{Ref}$



Lighting source of 3200°K
Imaging of colour signal A
⑮ pin $V_{B1} = V_{B0} + \alpha$
⑭ pin $V_{R1} = V_{R0} = V_{Ref}$



Lighting source of 3200°K
Imaging of colour signal B
⑮ pin $V_{B2} = V_{B1} + \beta = V_{B0} + \alpha + \beta$
⑭ pin $V_{R2} = V_{R1} = V_{R0} = V_{Ref}$

When white is imaged again in this state, white balance correction is not to be made.

Figure 6-2 (i). Inconvenience Caused when One Axis Correction Is Not Made

By repeating this in the same way, the range given by presetting (the outside frame portion surrounded by H and L in Fig. 6-2 (j)) is all covered, by which white balance correction is performed for almost all the colour signals.

After white balance correction is performed by means of B, if white is imaged again, white shifts to the outside of the area, making white balance correction impossible.

To prevent such an action, the diode and resistor are added to provide the following.

$V_{B2} - V_{R2} \leqq V_F$

Thus correction is made within the range of the shaded portion shown in Fig. 6-2 (j). (One axis correction)

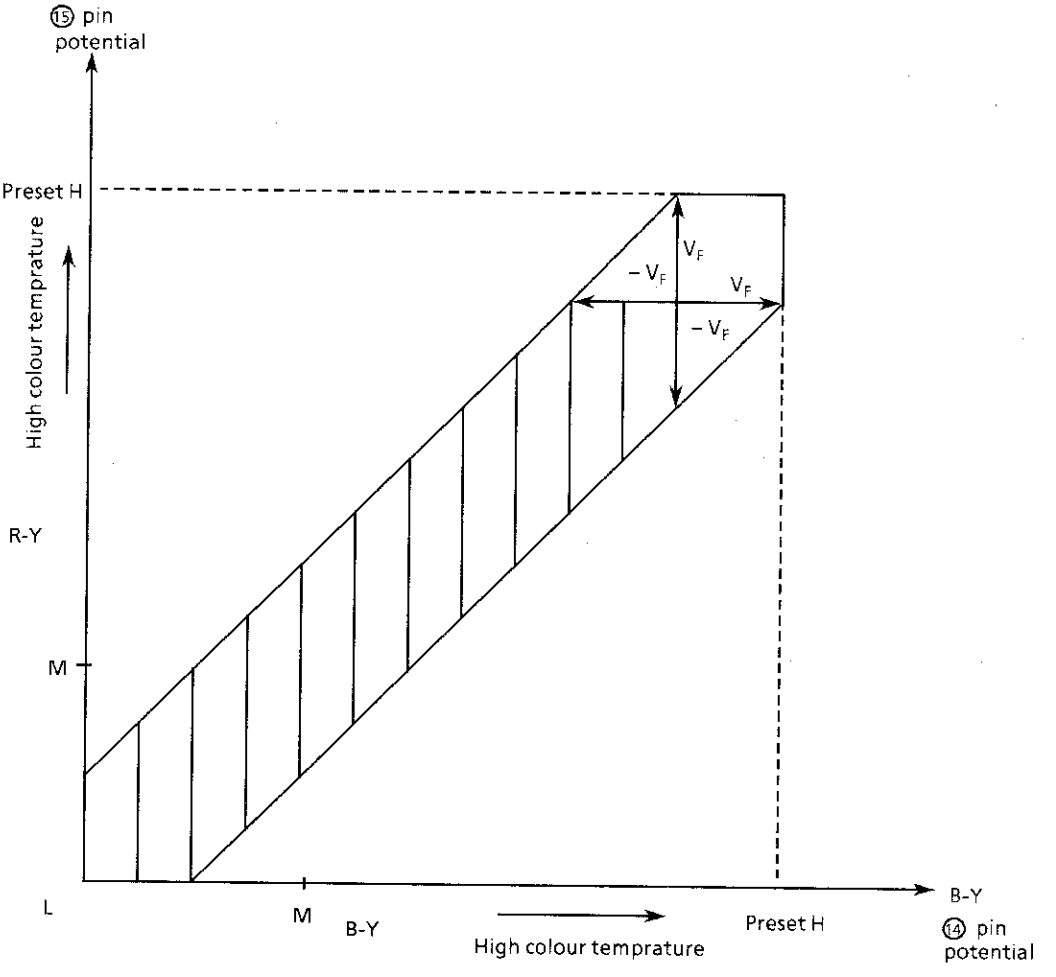


Figure 6-2 (j). White Balance Control Voltage Characteristics

4. White balance control

The control output pin (15) AWB B-Y CTL and pin (14) AWB R-Y CTL set as described above are buffered at IC302, after which the pin (14) buffer output is, as B-W/B (white balance control voltage of B-Y), resistance-mixed to pin (9) of IC201; the pin (7) output of IC302 is, as R-W/B (white balance control voltage of R-Y), resistance-mixed to pin (8) of IC201.

At high colour temperature, the colour differnece signal R-Y is decreased and the colour difference signal B-Y is increased. To correct this, the pin (7) output of IC302 is added to the R-Y gain setting terminal pin (16) of IC201, raining the gain of R-Y. Also, the pin (7) output of IC302 is reverse-amplified and its pin (8) output is added to the colour difference B-Y gain setting terminal pin (11) of IC201, reducing the gain of B-Y.

The white balance circuit is always AUTO. At adjsuting, by changing the pin (28) voltage of IC301, selection of preset, adjustment and writing in EEPROM are performed.

Pin (28)	Preset	Selected voltage (Pin NO.)	
		R-Y	B-Y
1/4 Vcc or less	AUTO	Time division of H~L	Time division of H~L
1/4 Vcc ~1/2 Vcc	M (3200°K adjustment)	Pin ⑫	Pin ⑱
1/2 Vcc ~3/4 Vcc	H (daylight colour temperature)	Pin ⑬	Pin ⑰

- 3200°K adjustment
  After getting in the camera adjusting mode, set the pin (28) voltage at 1/4 Vcc - 1/2 Vcc in a light source of 3200°K and select preset M.
  In the camera adjusting mode, perform white balance adjustment with CH04 and CH05 and write the data in the EEPROM.
- High colour temperature adjustment
  After getting in the camera adjusting mode, set the pin (28) voltage at 1/2 Vcc - 3/4 Vcc and select preset H. In a light source of 3200°K, using colour temperature conversion filter LB165, convert into high colour temperature. In the camera adjusting mode, perform white balance adjustment with CH14 and CH15 and write the data in the E^2PROM.
- Auto offset adjustment
  After getting in the camera adjusting mode, set the pin (28) voltage at 1/4 Vcc or less and select the auto mode. In a light source of 3200° K, make adjustment with CH12 and CH13 to correct the offset of IC301 and write the data in the E^2PROM.
  As the white balance is always in the auto mode, set the pin (28) voltage at 1/4 Vcc or less and write in the E^2PROM.

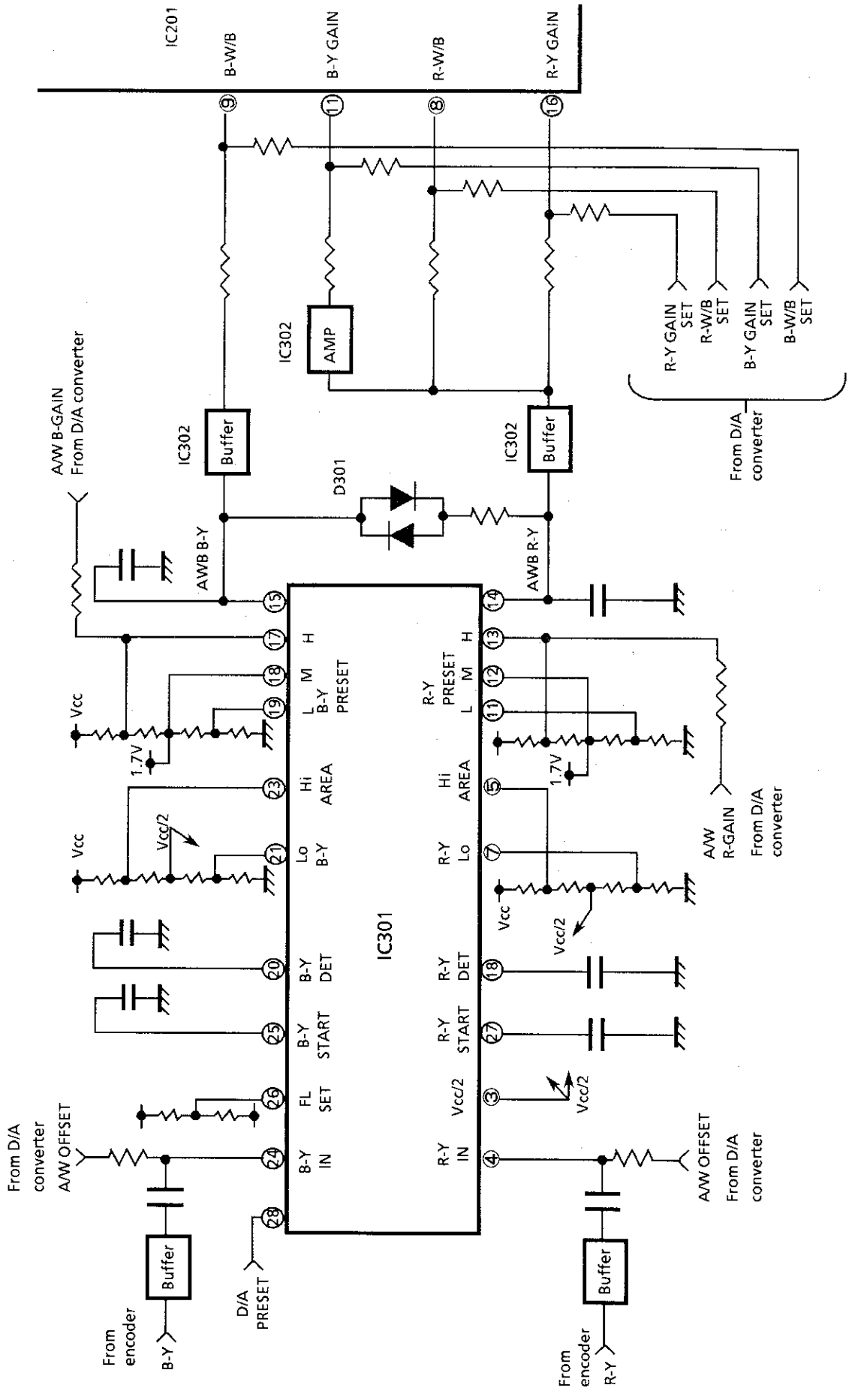


Figure 6-2 (k). Auto White Balance Section Circuit

7. AUTO FOCUS CIRCUIT

7-1. Outline: action of AF method of this unit

The AF method of this unit is image processing method. In this method, the principle is utilized that the clearer the outline of the object image in focus becomes, the more the high frequency component of the video signal increases.

After experiencing high frequency component extraction, A/D conversion and digital integration, the video signal is inputted in the AF microcomputer. Moving the focusing lens back and forth, the AF microcomputer calculates the increase and decrease of the high frequency component to judge how the object is out of focus. According to this judgement, it moves the focusing lens so that the high frequency component reaches its peak.

Not only the video signal but also the lens condition is utilized as information for focusing.

When the iris is stopped down, the depth of field becomes deep, making the change of high frequency component small. On the contrary, when the iris is opened, the depth of field becomes shallow, making the change of high frequency component large. Therefore, the focusing speed is controlled according to the position of the iris, improving the focussing accuracy.

When the zoom is on the telescopic side, the fluctuation of the video signal becomes large and the depth of field becomes shallow, making the change of high frequency component large. When the zoom is on the wide angle side, the fluctuation of the video signal becomes small and the depth of field becomes deep, making the change of high frequency component small. Therefore, the focusing speed is controlled according to the position of the zoom, improving the focussing accuracy.

As described above, the AF microcomputer drives the focus motor according to the condition of picture-taking by combining the main information based on the video signal with the above mentioned lens information.

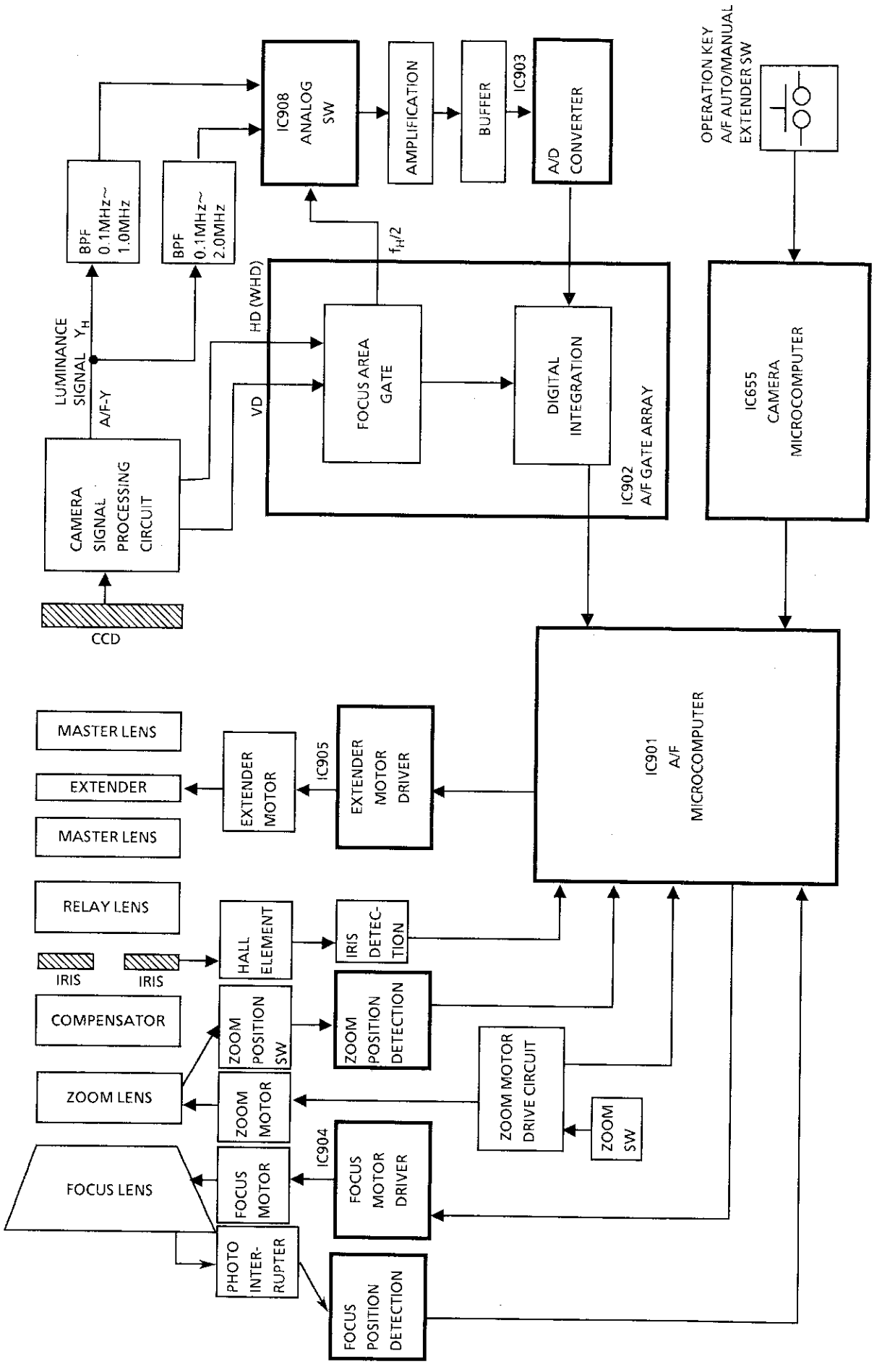


Figure 7-1. A/F System Block Diagram

7-2 Description of action

1. Filter circuit

In the auto focus circuit, the luminance signal Y_H (A/F-Y, P706 pin (1)) outputted from the camera processing circuit is used. In this signal, noise is reduced by synthesizing the signals of 0H and 1H.

After passing through the buffer (Q904), the signal is distributed to the two kinds of band pass filter (0.1 MHz~1.0 MHz, 1.0 MHz~2.0 MHz), where the high frequency component is ectracted. The band pass filter is the active filter composed of Q905, Q906, resistor and condenser.

The two kinds of signals passed through the filters are switched with a timing of $f_H/2$ by analog switch IC908, becoming the line sequential signal. Then, after passing through the amplification circuit (Q908) and buffer (Q911), the signal is sent to the A/D conversion circuit.

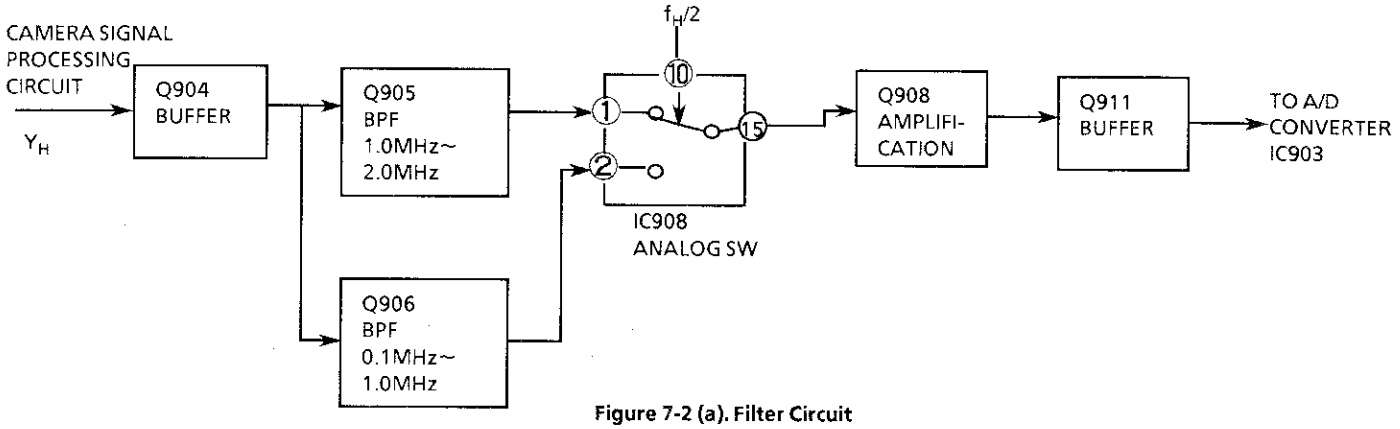


Figure 7-2 (a). Filter Circuit

2. A/D conversion circuit

The signal processed in the filter circuit is inputted in A/D converter IC903 pin (12). By means of the pin (10) and pin (11) terminal voltage, the range of A/D conversion is set (upper limit: 3.14 V, lower limit: 1.57 V). The reference voltage is obtained from the constant voltage circuit of IC909. This reference voltage (1.57 V) is also used for the bias voltage of filter circuit, etc.

The result of A/D conversion is outputted by means of the binary code (B1 - B6, B1 = LSB, B6 = MSB) and sent to A/F gate array IC902.

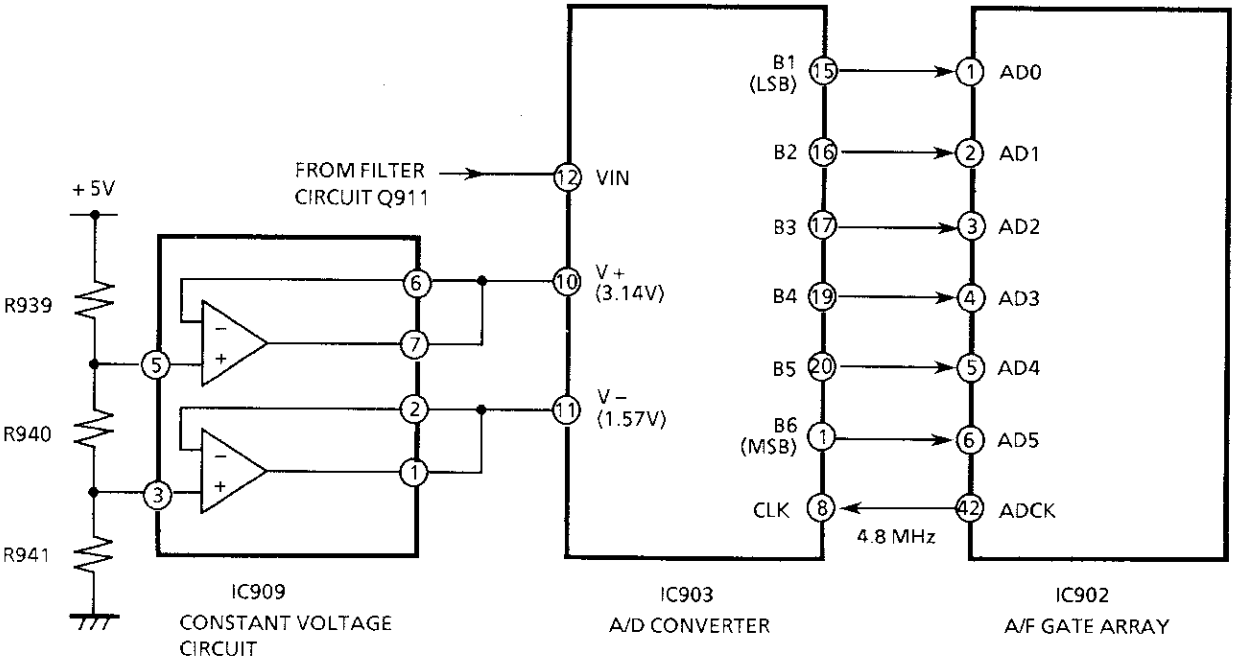


Figure 7-2 (b). A/D Conversion Circuit

3. Digital integration circuit

The signal having experienced A/D conversion at A/D converter IC903 is inputted in A/F gate array IC902, where the maximum value of the inputted data is stored for a period of 3V (digital integration). A/F microcomputer IC901 reads the result of integration with a timing of once per 3V (VD3 = "L") and performs focus action so that the value becomes maximum.

The low frequency data (0.1 MHz ~ 1 MHz) and high freqauency data (1 MHz ~ 2 MHz) are sent from the gate array to the A/F microcomputer by means of serial transfer (see Fig. 7-2 (c)).

Digital integration is performed in the area shown in Fig. 7-2 (d), where the two patterns are automatically changed and monitored according to the condition of the object and monitored.

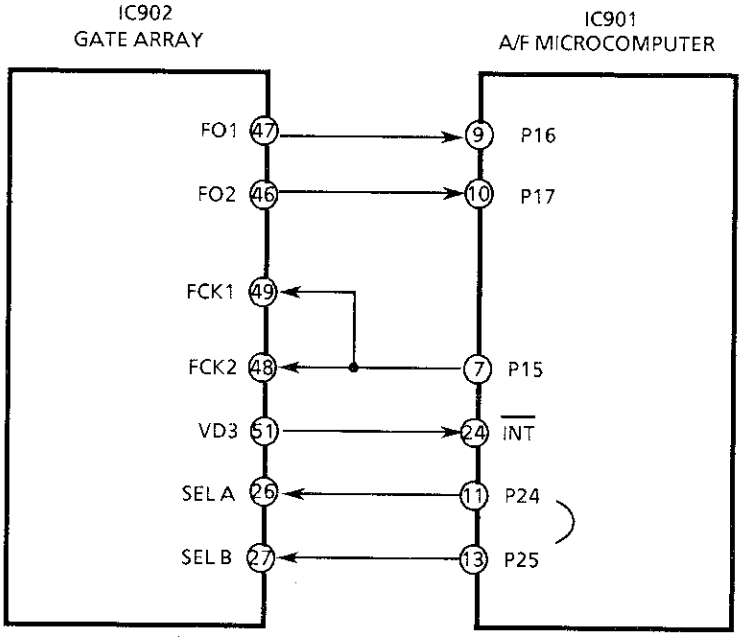


Figure 7-2 (c). Digital Integration Circuit

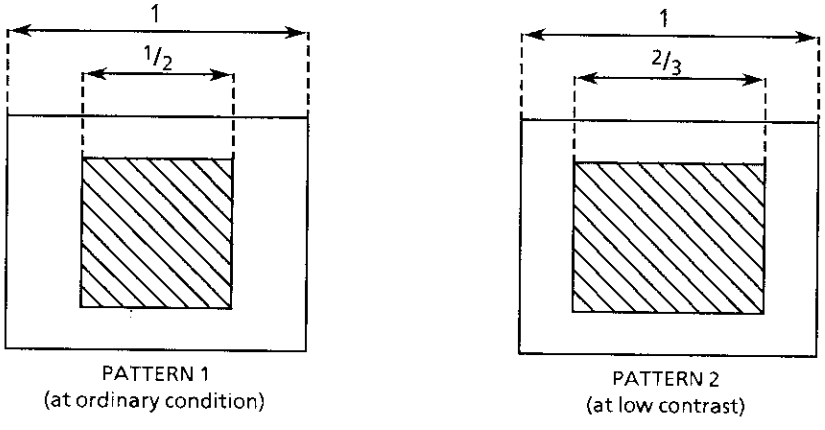


Figure 7-2 (d). Focus Area.

4. Focus motor drive circuit

A/F microcomputer IC901 drives the focus motor (DC motor) by using the 9 kinds of drive pulses (Fig. 7-2 (f)) having different duty ratios according to the condition of imaging. The drive pulses are synchronized with VD3 (3-dividing of VD, A/F gate array IC902 (51) output) and outputted from A/F microcomputer IC901 (14) (NEAR end direction) and (15) (INF end direction).

Receiving the drive pulses from the A/F microcomputer, focus motor driver IC904 drives the focus motor. Motor drive voltage section is made by adjusting the voltage applied to pin (5) by means of the volume (pin (9) is the constant voltage circuit output of + 5V). D903 and D904 are the damper diodes at starting of the focus motor. Pin (6) is the terminal for reset of the A/F microcomputer.

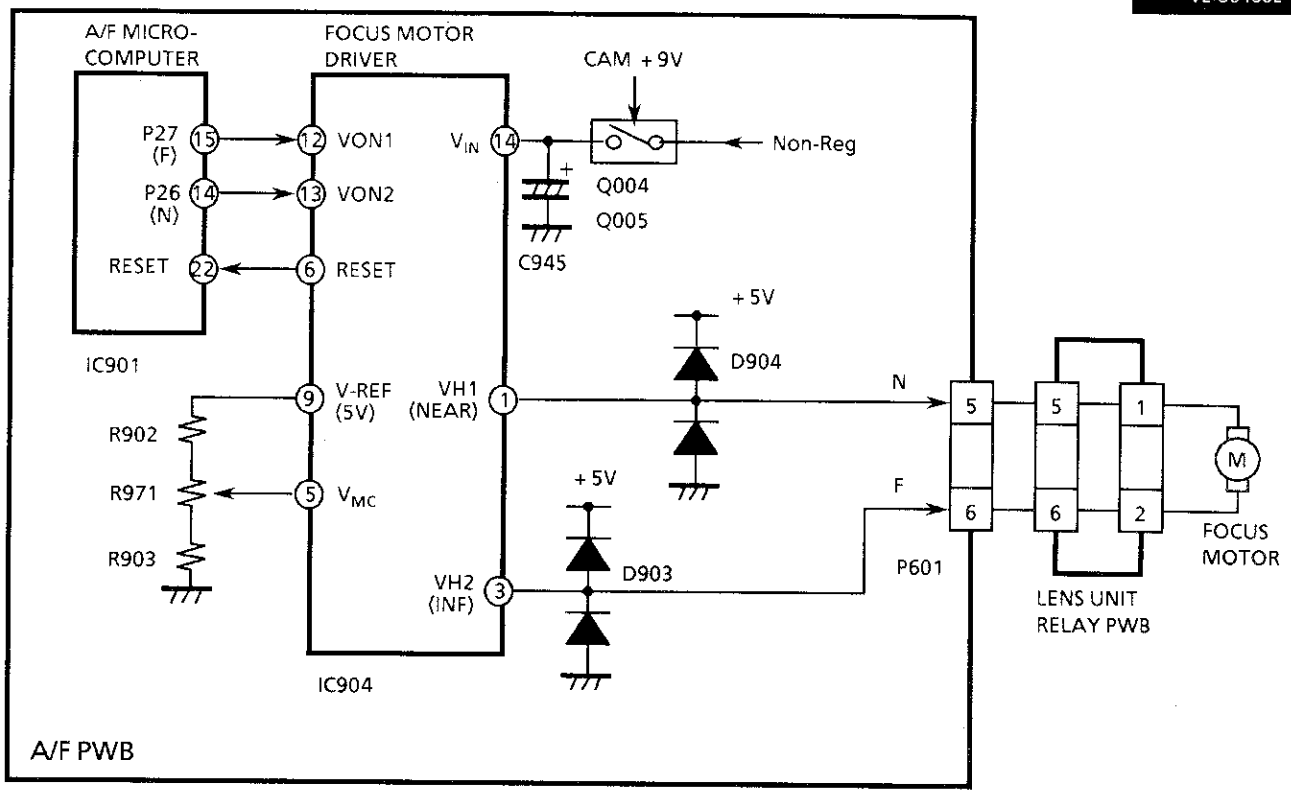


Figure 7-2 (e). Focus Motor Drive Circuit

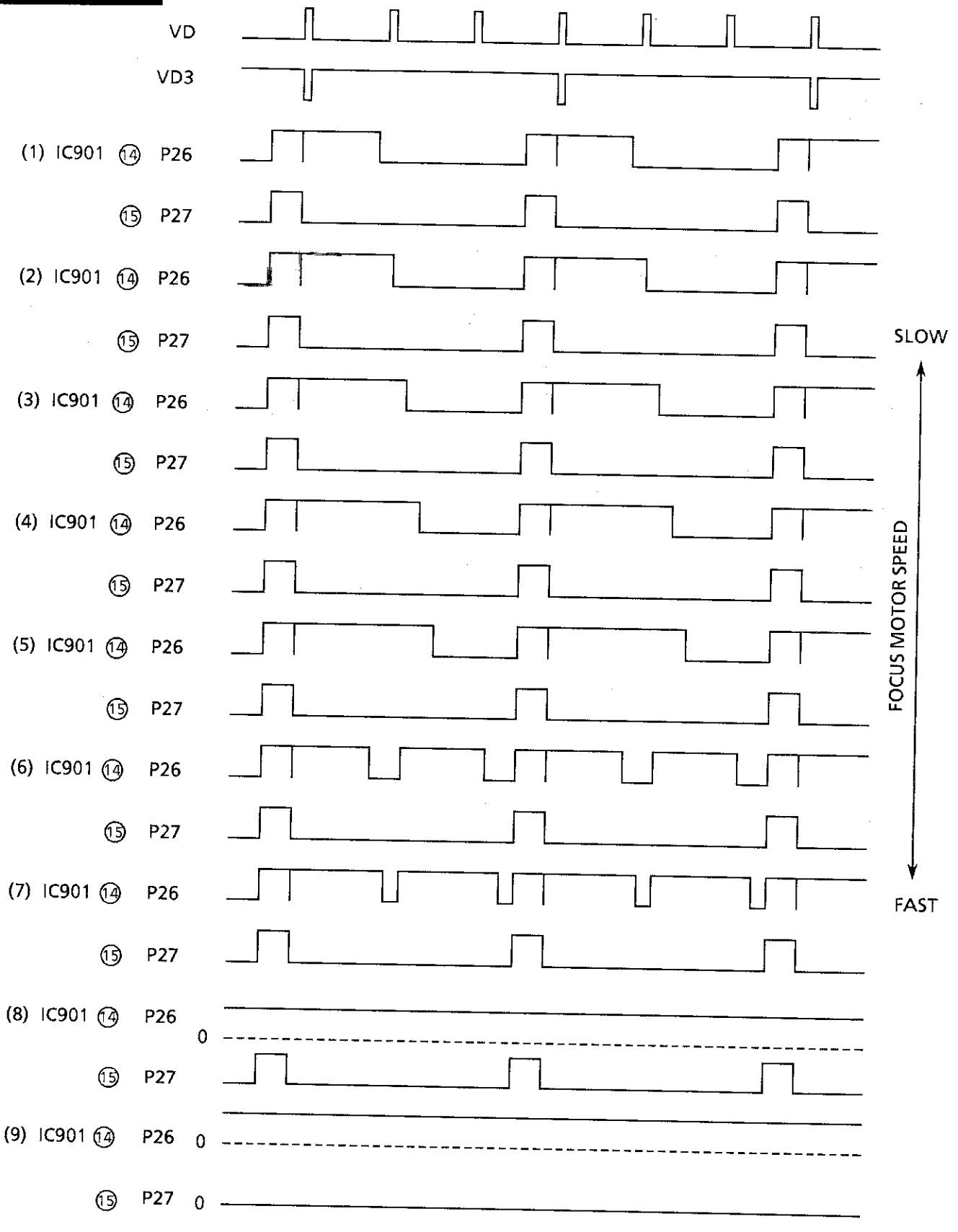
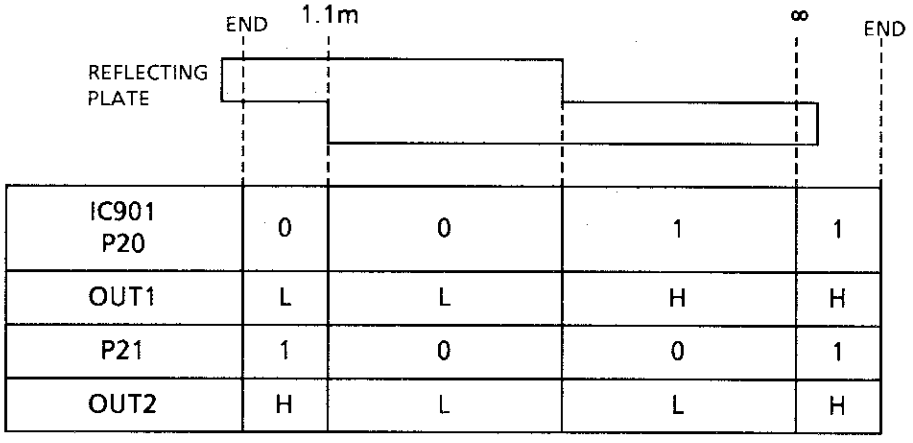


Figure 7-2 (f). Focus Motor Drive Pulse
(When the focus motor operating in NEAR direction)

5. Focus position detection circuit

Detection of the focus position is performed using the two photo reflectors and the reflecting plate stuck around the focus ring. The photo reflector output is inputted in comparator IC910 pin (3) and (5). The IC910 pin (1) and (7) outputs are sent to A/F microcomputer IC901 (39) and (40) respectively as focus position information. When the pin (40) input signal is "H", the A/F microcomputer judges that the focus lens is located at the end and reverses the rotating direction of the lens.



IC901 P20	0	0	1	1
OUT1	L	L	H	H
P21	1	0	0	1
OUT2	H	L	L	H

Figure 7-2 (g). Focus Position Detection Reflecting Plate Form and Output List

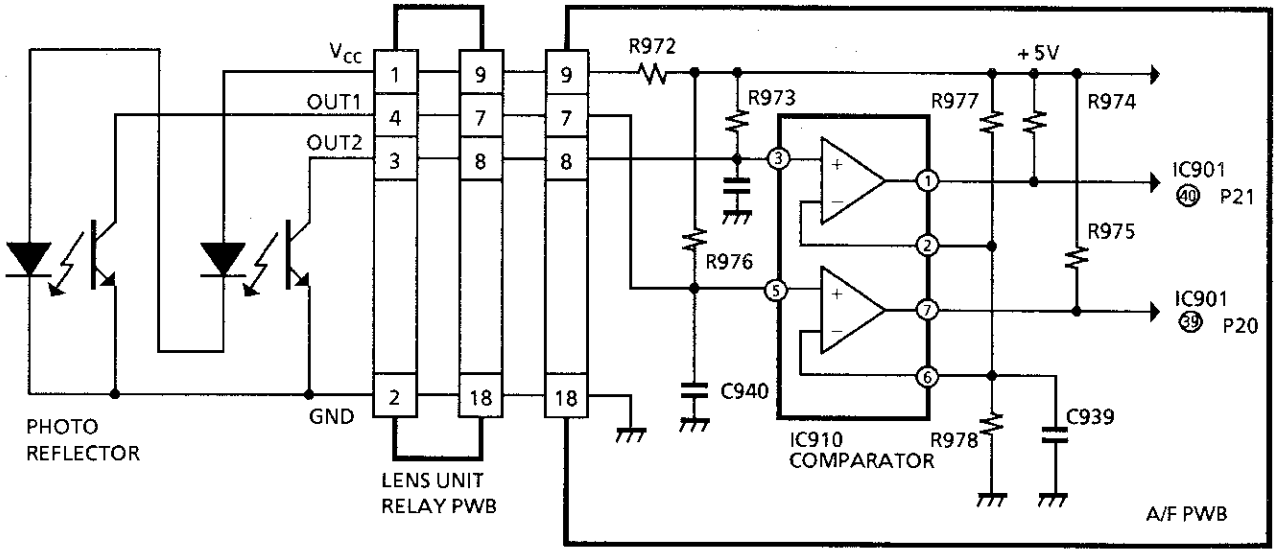


Figure 7-2 (h). Focus Position Detection Circuit

6. Iris position detection circuit

Detection of the iris position is performed by means of the hall element provided in the iris meter. D901 and R909 are used for protection of the hall element. The output signal of the hall element is amplified at IC907 (1). After experiencing offset adjustment at IC907 (2), the amplified signal is outputted from comparator IC906 at the two stages of low (when the iris is open) and High (when the iris is closed). (See Fig. 7-2 (j).)

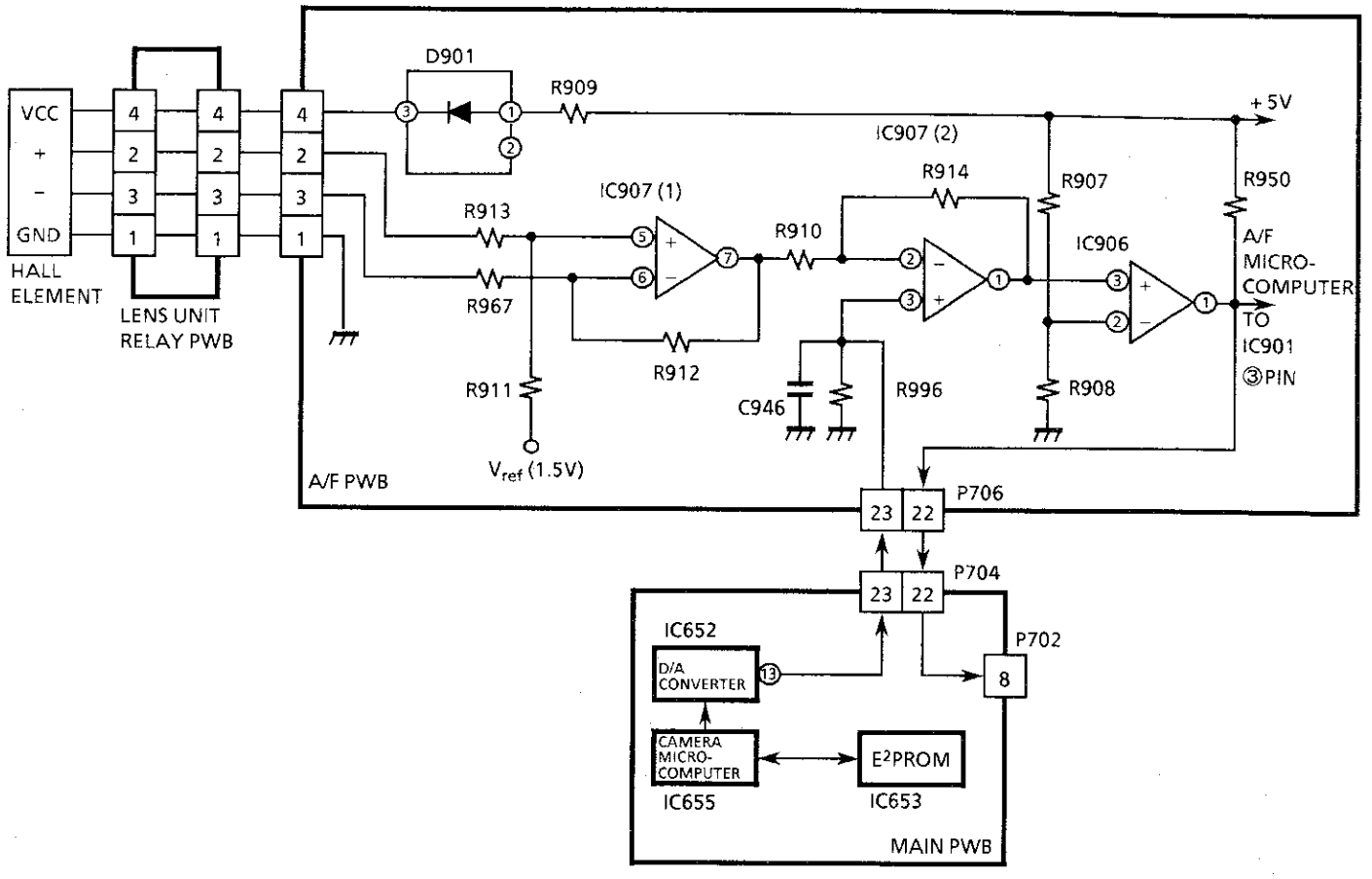
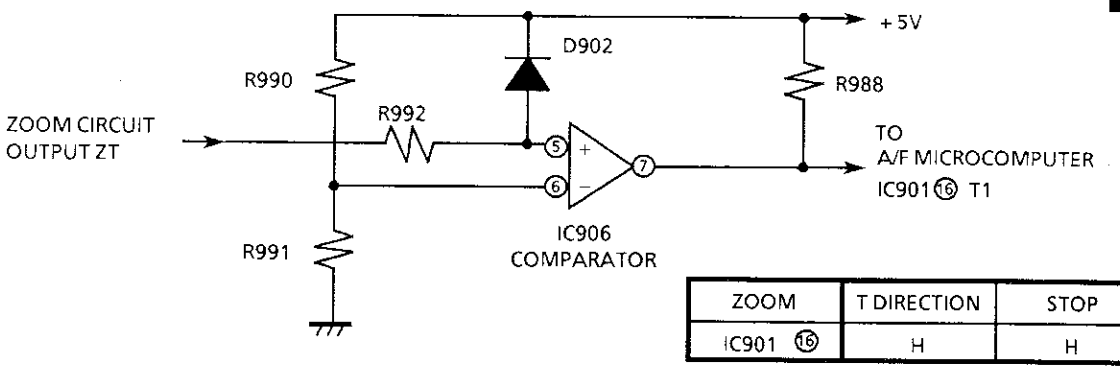


Figure 7-2 (i). Iris Position Detection Circuit

Figure 7-2 (j). Iris Position Detection Circuit Output

7. Zoom action detection circuit

In this unit, when the zoom ring is moved in the WIDE direction by operation of the zoom SW, focus action is stopped. When the zoom switch is not operated, the zoom motor drive citcuit output ZW and ZT (motor input terminal) are ordinarily of the same potential. However, when WIDE side operation of the zoom SW is performed, the potential of ZT is lowered (the potential of ZW is raised). This potential change of ZT is inputted in the comparator IC906 pin (5), where it is converted into the "L" and "H" signals and inputted in A/F microcomputer IC901 pin (16) T1.



ZOOM	T DIRECTION	STOP	W DIRECTION
IC901 ⑯	H	H	L

Figure 7-2 (k). Zoom Action Detection Circuit

8. Zoom position detection circuit

Zoom position detection is performed using the two micro SW. The micro SWs are switched by means of the convex and concave provided on the zoom ring, by which the output shown in Fig. 7-2 (l) is obtained. The output specification of the micro SW is shown in Fig. 7-2 (m) . The output of the SW is directly inputted in A/F microcomputer IC901 pins (41) and (42). When both the outputs of the micro SWs are "1", the A/F microcomputer judges that the zoom is in the macro area and stops focus action.

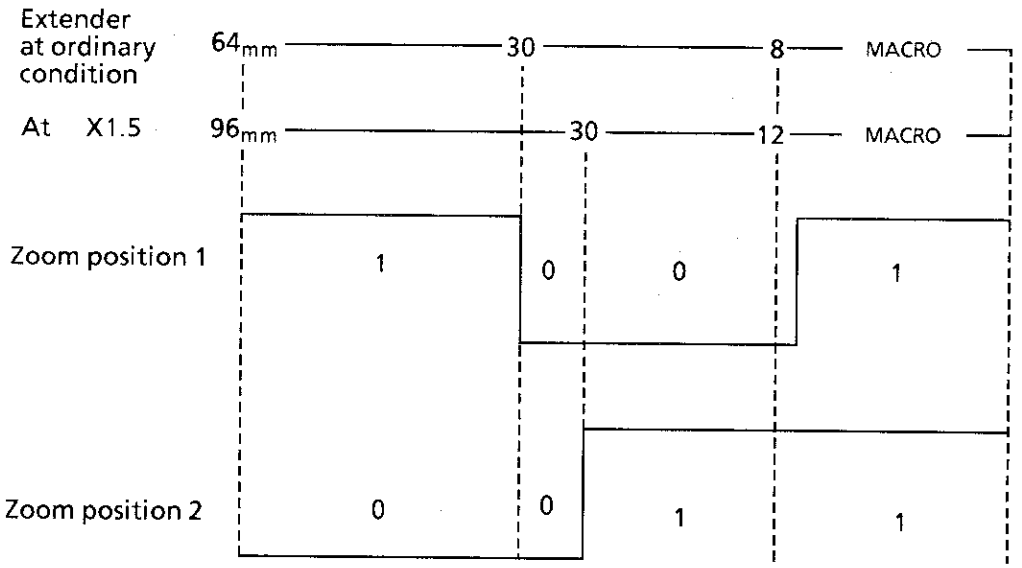
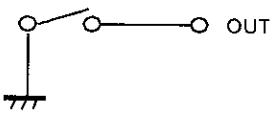


Figure 7-2 (l). Zoom Position Detection SW Output



SW	OUT
ON	0
OFF	1

Figure 7-2 (m). Zoom Position Detection SW Specification

9. Extender

Each time the extender SW of the operation PWB is turned ON, camera microcomputer IC655 pin (14) output "EXTENDER" is switched to "L" or "H". The A/F microcomputer detects these rise and fall with pin (4) P14 and outputs the "H" pulse to pin (37) (at rise) and pin (36) (at fall) for about 0.5 sec.

Extender motor driver IC905 rotates the extender motor in the same phase for 0.5 sec. to mvoe the extender lens to the 1.5 times side (at rise) or the ordinary magnification side (at fall) (see Fig. 7-2 (n)). IC655 pin (37) output "EXT MODE" is used for preventing the extender from acting inadvertently when the power is turned ON or the camera mode and VCR mode are changed. When "EXT MODE" is "L", the A/F microcomputer does not detect the rise and fall of "EXTENDER".

Using camera microcomputer output pin (14) "EXTENDER" and pin (37) "EXT MODE" as input, A/F gate array IC902 switches the output of the "EXT OUT" signal which displays in the view finder the frame showing that the extender is of ordinary magnification (see Table. 7-2 (b)).

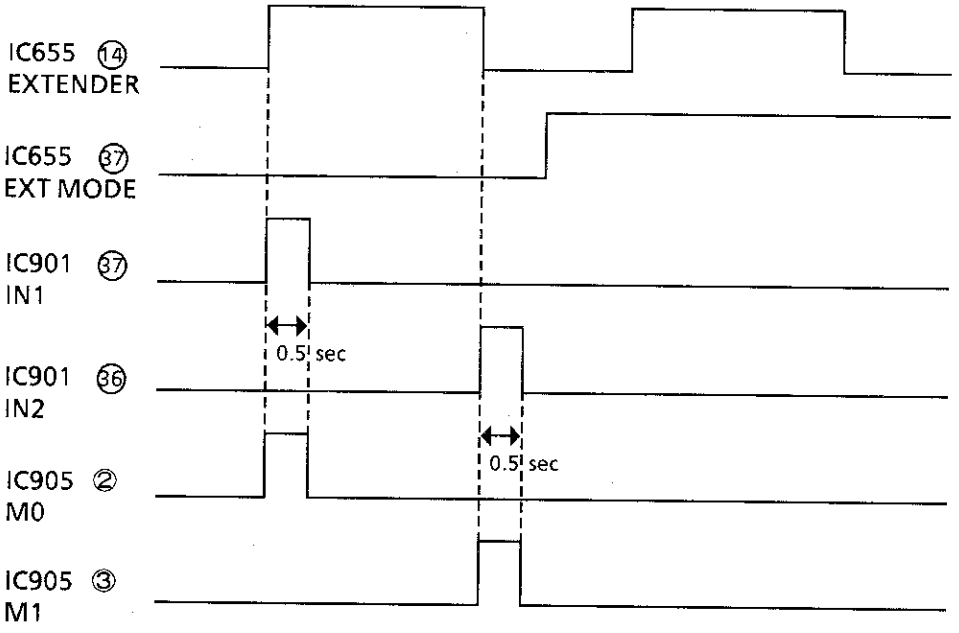


Figure 7-2 (n). Extender Drive Timing

D0	L	H	L	H
D1	L	L	H	H
M0	L	H	L	L
M1	L	L	H	L
MODE	OPEN	NORMAL ROTATION (×1.5)	REVERSE ROTATION (NORMAL)	BRAKE

Table 7-2 (a). Extender Motor Driver IC905 Logic List

EXTG-1	H	L	H	L
EXTG-2	H	H	L	L
EXT OUT	×	○	×	×

○ : Outputting gate frame
× : Not outputting gate frame

Table 7-2 (b). A/F Gate Array IC902 Extender Gate Frame Display Logic List

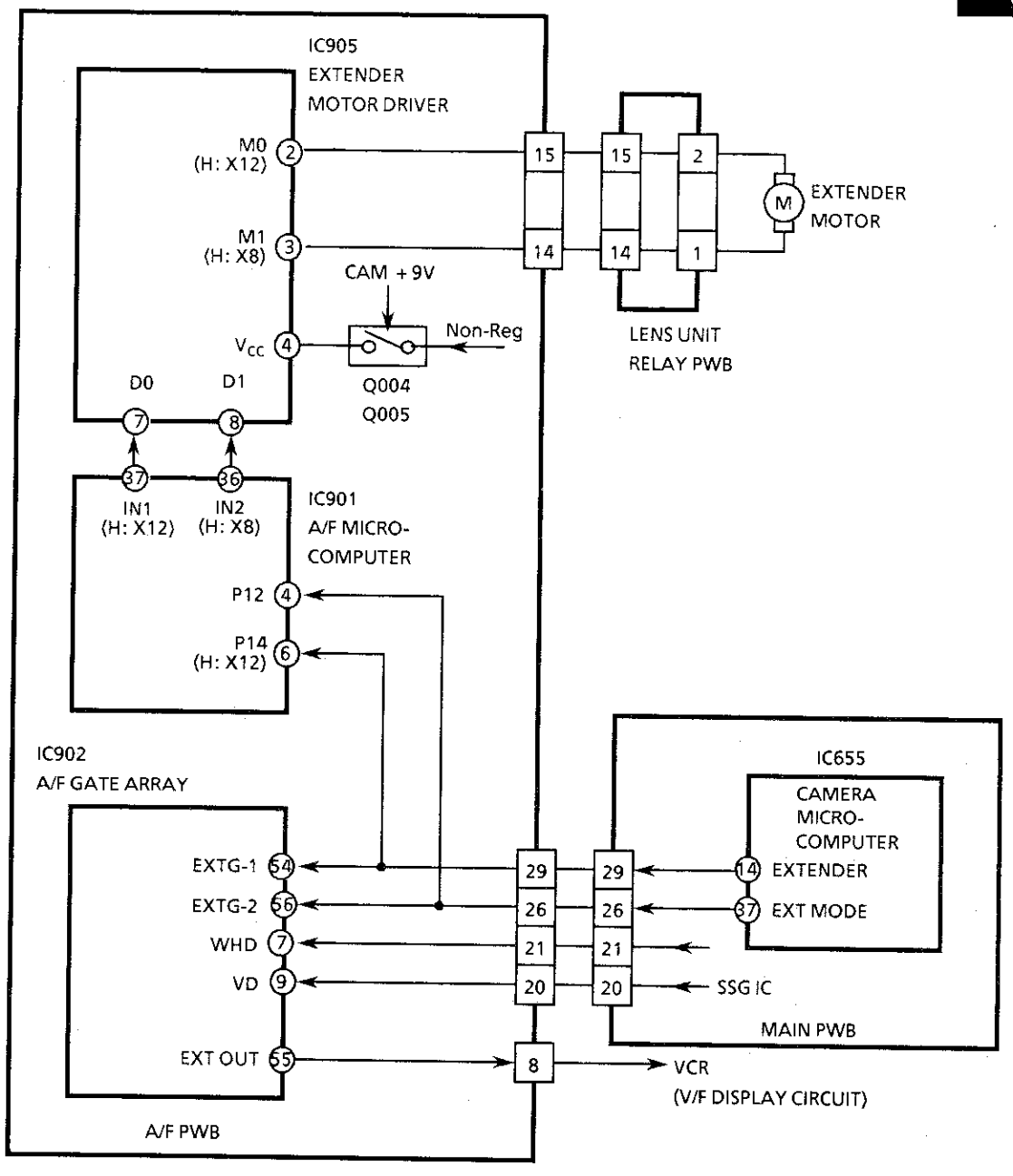


Figure 7-2 (o). Extender Motor Drive Circuit and Extender Gate Frame Display Circuit

VL-C780S/H/X
VL-C7400E
VL-C690S/H/X
VL-C6400E

SHARP

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